NIRSPEC

UCLA Astrophysics Program **U.C. Berkeley** **W.M.Keck Observatory**

George Brims **Created March 28, 1997**

NIRSPEC Software Design Note 21.00 - Clock generator software

Introduction

The clock generator transputers produce clocking patterns for the two detector arrays. Although there are marked differences between the two arrays, the overall architecture of the software is the same for each. The only thing that changes is the actual clock pattern sent out, and the number of detector sampling modes supported.

Background - hardware details

The DAQ17 clock generator/motor control boards (see NEDN17 for more details) each have a single transputer, with memory-mapped I/O ports for clocking arrays, driving stepper motors, and general digital control and monitoring. Writing to or reading from the hardware ports is simply a matter of assigning values to, or reading them from, specific locations. Occam allows you to PLACE a variable at a specific hardware address.

The clock output port is 32 bits wide, and passes through a 16k deep FIFO buffer. The unique (I think) feature of the DAQ17 clock generators is the use of the re-transmit feature of the FIFO buffers. The total number of clock words required to scan through one of these arrays is huge, but for the most part the pattern is actually very repetitive. The hardware implementation allows us to load a repeating section of data into the FIFO buffer, assign it a repeat count, then trigger output. The hardware sends out the whole sequence the assigned number of times without program intervention. Data output from the FIFO is precisely timed by a hardware clock, and can also be much faster than the transputer can achieve by direct output. Of course sometimes (such as the start and end of a clocking sequence) the output required is something that doesn't repeat. In this case the transputer will write directly to the output port via a different register