Frank Henriquez & George Brims **May 7, 1996**

NIRSPEC Electronics Design Note 17.01 - DAQ17 Description

Introduction

The DAQ17 transputer board performs two functions. It is used as the clock generator for the infrared arrays, and it also has multiple parallel I/O ports which can be used for stepper motor driving, switch sensing and general digital control and monitoring. The DAQ17 was designed and built by DSP Systems, after extensive reviews of our proposed architecture, which evolved from the system running the Gemini twin-channel infrared camera. The design is based on two boards used in Gemini; the motor controller and the clock pulse generator. These two boards were so similar architecturally it seemed reasonable to combine them, and in fact this was achieved with real estate to spare. One advantage of combining the two boards is more efficient provision of spares. There will be a total of about six DAQ17s in the system, with one spare which can be substituted for any of the others.

Functional description

Each DAQ17 board has one T805 Transputer running at 25MHz, with 4 MBytes of RAM. Logic programmed into FPGAs is used to interface the CPU to I/O functions. Various buffers are mapped into the memory space of the processor, so that writing or reading digital data is as simple as assigning or copying a variable. The logic can also interrupt the processor when needed for synchronization of events. Details of this process are explained in the software design notes.

For clock generation, the DAQ17 transputer writes out via two 16 bit wide FIFO buffers with software selectable speeds. These FIFOs feed two output connectors; the 8 least significant bits are also taken to pins on the VME backplane so they can be passed to the acquisition boards. The FIFO buffers, normally run synchronized, are used in a repeating mode to take advantage of the repetitive nature of the clock waveforms for detector arrays. Data which isn’t repetitive can be written to the output through a direct register, bypassing the FIFO buffers.

In addition to the clock outputs, each board has four 8 bit output ports, the "motor" ports, and four 8 bit input ports, called ?status” ports. These come out on four DB25 connectors, one motor and one status port together on each. The status ports are always inputs, but the motor ports can be modified to act as bidirectional (input and output) ports if more inputs are needed.

The motor port output can be automatically terminated by a "watchdog" timer; this sets the output on the motor port to all zeros. Since one of the bits controls the power on/off of our API stepper motor drivers, this powers down the driver. The motor port bits also default to the off state when we power up the boards. This feature is based on our experience with the Gemini motor

controller. Most of our stepper motors are inside the cryogenic environment, so they need to be powered down whenever they are not being driven to minimize heat input into the dewar.

In addition to the transputer and logic on the board, there was room to put in a dual TRAM[1] slot for the addition of off-the-shelf transputer interface modules. We will use some of these slots for the fiber-optic interface to the host and to add RS232 capability.

Hardware details

The boards are implemented in VME format, allowing us to use standard Eurocard packaging, connectors, and other hardware. The DAQ17 connects only to power and ground signals on the VME bus. One could insert a DAQ17 into a VME-based computer, but it would not interact in any way with that system!

Links

The T805's links appear on the 96 pin DIN connectors at the rear of the board (J2A and J2C) as listed in Table 2. The speed of these links are selectable, link 0 separately but the other three only as a group. The link speed is controlled by a DIP switch, labeled S1, allowing 8 possible speed combinations. The speeds for each setting of S1 are listed below.

Link0	20MHZ	20MHZ	10MHZ	10MHZ	10MHZ	10MHZ	5MHZ	5MHZ
Link123	20MHZ	10MHZ	20MHZ	10MHZ	10MHZ	5MHZ	10MHZ	5MHZ
Switch 1A	off	off	off	off	on	on	on	on
Switch 1B	off	off	on	on	on	on	off	off
Switch 1C	off	on	off	on	on	off	on	off

Table 1 Link Speed Switch Settings

The DAQ17 has two 96 pin connectors (J1 and J2) at the rear of the board, so it can be inserted in a standard VME backplane. The link connections are made through uncommitted pins on the J2 connector to the backplane, which are joined by wirewrapped connections to form our transputer network. Note that while the pinouts look similar to the DAQ15, the DAQ17 pinouts are actually quite different. The two board types cannot be swapped!

In the table below, you will note there are three sets of links listed. The links on the A column are for the on-board transputer, while the others connect to the dual TRAM sockets to connect any transputers plugged into there. The subsystem signals on A30-A32 are also for the primary transputer, while those on A27-A29 connect to the TRAM site. Spl0 - Spl7 are the eight least significant bits of the clock output, also seen at the front connector.

[1] TRansputer Application Module - a standard daughterboard format for transputers packaged with various kinds of interfacing such as RS232 or SCSI.

	J2A	J2C	
1	ground	ground	
2	unused	unused	
3	LinkOut1	LinkOut1	These are for the TRAM site furthest from the board
4	LinkIn1	LinkIn1	edge.
5	ground	ground	
6	ground	ground	
7	unused	unused	
8	LinkOut2	LinkOut2	
9	LinkIn2	LinkIn2	
10	ground	ground	
11	LinkOut0	LinkOut0	
12	LinkIn0	LinkIn0	
13	LinkOut3	LinkOut3	
14	LinkIn3	LinkIn3	
15	unused	unused	
16	ground	ground	
17	unused	ground	
18	Spl0	unused	
19	Spl1	LinkOut1	These are for the TRAM site nearest the board edge.
20	Spl2	LinkIn1	
21	Spl3	ground	
22	Spl4	ground	
23	Spl5	unused	
24	Spl6	LinkOut2	
25	Spl7	LinkIn2	
26	unused	ground	
27	notSubReset	LinkOut0	
28	notSubAnaylse	LinkIn0	
29	notSubError	LinkOut3	
30	nReset	LinkIn3	
31	nAnaylse	unused	
32	nError	ground	

Table 2 DIN-96 Link pinouts (see DAQ17 Schematics, pg 2 of 10).

DAQ17 Input/Output Ports

The DAQ17 uses two Field Programmable Gate Arrays (FPGAs) to split the 32 bits of input and 32 of output into four pairs of 8 bits. The I/O appears on four stacked DB-25 male connectors. Each connector has 8 output bits and 8 input bits plus 5 volts and ground, which can be used to power remote ISO150 isolators. The output data bits (Motor) are labeled MDD0 through MDD31 and the input data bits (Status) are labeled SD0 through SD31.

Pin#	P1A	P2B	P2A	P2B
1	MDD0	MDD8	MDD16	MDD24
2	MDD2	MDD10	MDD18	MDD26
3	MDD4	MDD12	MDD20	MDD28
4	MDD6	MDD14	MDD22	MDD30
5	GND	GND	GND	GND
6	+5V	+5V	+5V	+5V
7	SD0	SD8	SD16	SD24
8	SD2	SD10	SD18	SD26
9	SD4	SD12	SD20	SD28
10	SD6	SD14	SD22	SD30
11	GND	GND	GND	GND
12	+5V	+5V	+5V	+5V
13	nPortOE0	nPortOE1	nPortOE2	nPortOE3
14	MDD1	MDD9	MDD17	MDD25
15	MDD3	MDD11	MDD19	MDD27
16	MDD5	MDD13	MDD21	MDD29
17	MDD7	MDD15	MDD23	MDD31
18	GND	GND	GND	GND
19	+5V	+5V	+5V	+5V
20	SD0	SD9	SD17	SD25
21	SD2	SD11	SD19	SD27
22	SD4	SD13	SD21	SD29
23	SD6	SD15	SD23	SD31
24	GND	GND	GND	GND
25	+5V	+5V	+5V	+5V

Table 2 DAQ17 I/0 Connector pinouts. See Schematics pg 8 of 10.

Motor (Output) Port Description

Each of the I/O port FPGAs (labeled **Daq17_2.tdf** and **Daq17_3.tdf** on the schematics, page 7 of 10) handles 16 bits of I/O data. The Motor output bits (MDD0 - MDD15 and MDD16 - MDD31) are buffered by 7438 TTL open collector buffers; the outputs of the 7438s have pullup resistors and lead directly to the output connectors. In this configuration, the port can **only** be used for output, with high current drive capability. See page 8 of 10 of the schematics for the 7438 locations.

Since the 7438 is a unidirectional buffer, the output port cannot be used as a bidirectional port (or an input port) without a simple hardware modification. Removing the 7438 allows the FPGA output bits to be used as an input port. To reduce the risk of damaging the FPGA, the 7438 **must** be replaced by an inline resistor pack (labeled SIP4ISO-33, RP9 - RP16).

The 7438 is a 4 bit device; there are 8 devices on the board. Since there are 32 output bits, each port can be used as an:

- 8 bit output port
- 8 bit input (or bidirectional) port
- 4 bit output, 4 bit input (or bidirectional) port

Examples of how to use the output port are in our occam test code, in procedure dac.write. This routine writes to the DAC on the A/D offset board. There are also routines to drive Dallas Semiconductor DS1820 temperature sensors; these demonstrate how to use the motor port as a bidirectional port. Note that this motor port has been modified to act as a bidirectional port. **This type of modification needs to be taken into account when putting a spare board in place.**

Status (Input) Port Description

The Status Port bits share the same connectors as the motor output bits. There's nothing remarkable about their operation. The motor control code, which includes reading switch values, has examples on how to read the switches.

FIFO (Clock) Port Description

The DAQ17 has two 16 bit by 16K FIFO ports, which can be used independently or as a single 32 bit by 16K FIFO (schematics pg. 4 of 10). The output of the FIFOs is controlled and directed by two FPGAs, labeled **DAQ17_6.tdf** and **DAQ17_6.tdf** on schematics pg. 9 of 10. The FIFOs can be clocked at up to 50 MHz; this rate can be controlled via software.

The FIFO data appears on two stacked DB-25S female connectors. When looking at the front of the DAQ17 (with the I/O and FIFO connectors) the left FIFO DB-25 supplies the lower 16 bits of the FIFO data. The upper 16 bits appear on the right hand FIFO DB-25. The lower 8 bits (DataOut0 - DataOut7) of the data stream are buffered and redirected to the backplane, where they appear as Spl0 - Spl7 on the 96 pin DIN connector, J2a. The Splx bits are a duplicate of the bits on the front connector. These bits can be used to pass signals along the backplane. In this application we use DataOut7 as the DAQ15 FIFO Write signal, which tells the DAQ15s to read in each set of pixel data from the A/D converters.

The A/D Convert and A/D Select bits are also generated as part of the clock waveform, as DataOut16 and DataOut18. They are brought out to two BNC connectors on the front panel, and from there go to the offset board in the analog crate. We chose these particular data bits for convenience in picking off the signals from the back of the stacked DB25 connector (they also appear on the DB25).

The pinouts for the two DB25 connectors are given below.

Pin#	DB25 Left	DB25 Right
1	DataOut0/SPL0	DataOut16
2	DataOut2/SPL2	DataOut18
3	+5V	+5V
4	DataOut4/SPL4	DataOut20
5	DataOut6/SPL6	DataOut22
6	+5V	+5V
7	DataOut8	DataOut24
8	DataOut10	DataOut26
9	+5V	+5V
10	DataOut12	DataOut28
11	DataOut14	DataOut30
12	+5V	+5V
13	CONNSIG	CONNSIG
14	DataOut1/SPL1	DataOut17
15	DataOut3/SPL3	DataOut19
16	GND	GND
17	DataOut5/SPL5	DataOut21
18	DataOut7/SPL7	DataOut23
19	GND	GND
20	DataOut9	DataOut25
21	DataOut11	DataOut27
22	GND	GND
23	DataOut13	DataOut29
24	DataOut15	DataOut31
25	GND	GND

Other DAQ17 Features

The FPGAs also have diagnostic LEDs which can be used to test the software. There are examples of their use in our code.