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NIRSPEC Electronics Design Note 16.02 - Transputer backplane wiring

1 Introduction

The NIRSPEC transputer boards[1] plug into a standard VME backplane. The backplane is not used as a VME bus in the normal way; rather it's used as a convenient way to provide power and ground to the boards. We can also use standard hardware (connectors, card cages etc.) in the 19" form factor. Another advantage of using VME is that the VME backplane has a lot of uncommitted pins on the P2 connector. The transputer links and subsystem signals are brought out to these uncommitted pins, where we can link them up as we need to, using wirewraps for permanent connections, and jumper cables for temporary links. This note describes the physical layout of the transputer network, and all of the interconnections on the backplane.

2 Transputer network layout

The host computer (a Sparcstation) interfaces to the transputer system using a unit called a Matchbox, made by Transtech. The Matchbox interfaces to the external SCSI port of the host computer. Coupled with the Transtech driver software, the Matchbox gives us a single transputer serial link to the first of the front end transputers. It is important to note that transputer links are *not* RS232, RS422 or any other standard that can be used over long distances. They are TTL level signals, only reliable over a few feet, such as inside our cabinet, so we convert them from TTL to fiber-optic signals and back in order to cover the distance to the electronics cabinets at the instrument. The fiber-optic system comprises two TRAMs[2], and is completely transparent to the software.

The link from the host goes to the first transputer in the front end system, known as the root transputer. The function of the root transputer is to act as a router for messages from the host computer to the transputers, and for data going back.

As well as acting as root (a fairly trivial job), this transputer is the housekeeping transputer which monitors things like cabinet and dewar temperatures, and is housed in its own separate box, so that it can control power to the rest of the front end system. The single link from the host connects

[1] DAQ15 and DAQ17, described in NEDN15 and NEDN17 respectively. DAQ15s acquire data from the A/D converters, and DAQ17s are used for clock generation, motor control and housekeeping.

[2] **TR**ansputer **A**pplication **M**odule - a standard transputer daughtercard format.

to link 3 of the root transputer. There are two camera systems plus a number of motor controllers, so our network has three branches emanating from the root transputer on links 0, 1 and 2.

The transputer network layout is shown in Figure 1. As we go from the host to the root transputer, then along each branch, note that the "upstream" link is link 0, and the "downstream" link is link 1. There is nothing special about any link; in fact they are completely identical except for the numbers. We merely chose this convention to keep things simple when writing the software. The transputer software protocol for the two camera sections mandates a couple of other simple conventions. First of all the clock generator transputer is nearest the host, since it passes on some messages, but not others, to the acquisition transputers (for instance a "go" message has meaning to the acquisition transputers but an "itime" does not). Secondly, the last acquisition transputer in each camera section has its "downstream" link looped back to link 2 of the clock transputer. This makes some of the message passing and handshaking simpler.

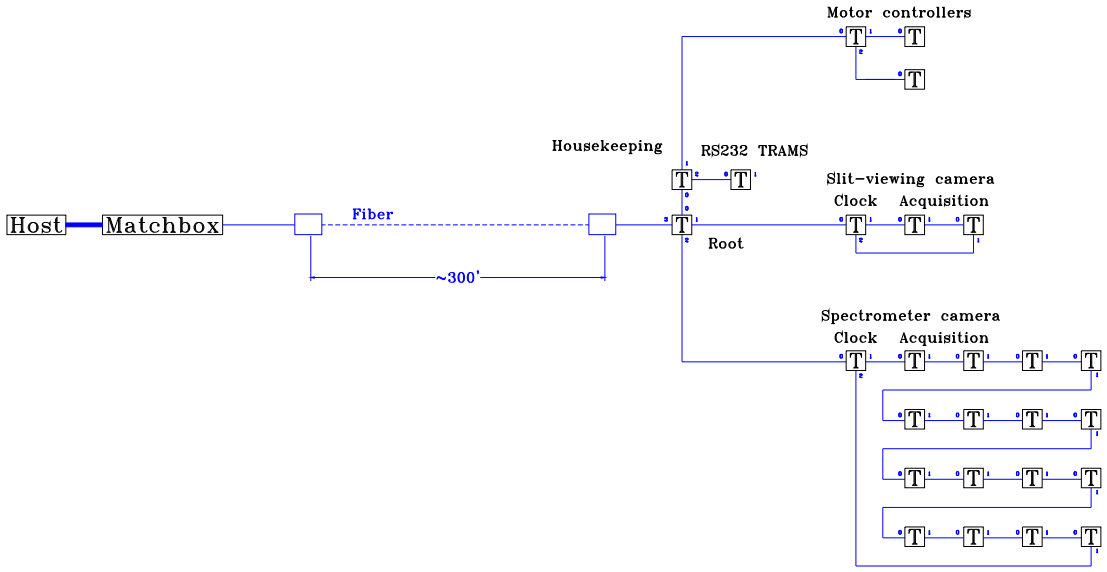

Figure 1: Transputer link layout

In addition to the links, there are a set of subsystem signals which go from the host computer to every transputer in the network, allowing the host computer to reboot and download software to the transputers, and to monitor for errors.

There are also logic signals (not links) which are passed along from the clock generator to the acquisition transputers in each camera section. These signals are generated as part of the clock output which drives the detector arrays, and trigger the acquisition transputers to read data from the A-D converters on the analog boards.

3 Hardware details

The details of the connections are shown in Figure 2 and listed in the tables at the end of this section. All the links across the backplane are implemented using wirewraps. Each transputer serial link comprises two wires, since the links are bidirectional. Subsystem signals (see below) are each on a single line daisy-chained along all the occupied slots. The data read signals are also on single wires.

3.1 Root transputer to backplane connections

The connection between the housekeeping transputer crate and the main transputer crate is via a straight through DB37 twisted-pair cable. The DB37 connector is mounted just behind the backplane. For our early tests we connected the crate straight to the Matchbox without the separately housed root transputer. We then made the housekeeping transputer's connector pinout the same as the Matchbox, as far as possible. Links 0, 1, and 2 from the housekeeping transputer are on the same pins as links 0, 1, and 2 from the Matchbox (the Matchbox has four links, although the driver software has a single-user license so we can only use one at a time). The subsystem signals are on the same pins as the link 0 set on the Matchbox (the Matchbox has separate sets for each link so it can support 4 completely separate transputer networks).

3.2 Backplane links

The two types of transputer board (DAQ15 and DAQ17) have four transputers and one transputer respectively. There are no built-in links between the four on the DAQ15, so even the transputers on that style of board have to be connected to each other via the pins on the backplane.

In the motor controller section, which is a series of DAQ17s only, we just daisy-chain from link 1 of one board to link 0 of the next in line. There is no loopback at the end of the branch as in the camera sections. We have installed links for up to five motor controller boards, although we only have plans at the moment to install three in the crate.

In the slit-viewing camera section, we only use one of each type of board, and only two of the DAQ15's four transputers. We connect link 1 of the clock generator transputer (the DAQ 17) to link 0 of the first DAQ15 transputer (designated transputer A), link 1 of transputer A to link 0 of transputer B, and then from transputer B's link 1 back to the clock generator transputer's link 2.

In the spectrometer camera section, we do exactly the same, except that in this branch we have 4 DAQ15s, numbered 1 to 4, each with transputers A through D. We connect from link 1 of transputer 1D to link 0 on transputer 2A, and so on down the line. Again link 1 of the last acquisition transputer (4D) links back to link 2 of the clock generator.

3.3 Subsystem signals

In addition to the links there are three “subsystem” signals (reset, error and analyse) which must go to all the transputers. These are just three wires which daisy chain from board to board. The DAQ15 and DAQ17 boards have these signals on the same pins, and in the same order from top to bottom (reset, analyse, error), which makes the layout pretty simple.

3.4 Data read signal

In addition to all the transputer link and subsystem signals, there are also signals which need to pass from the clock generator (DAQ17) to the acquisition board(s) in each camera section. These signals are part of the clock waveform, and they tell the acquisition boards when to read data into their FIFO input buffers.

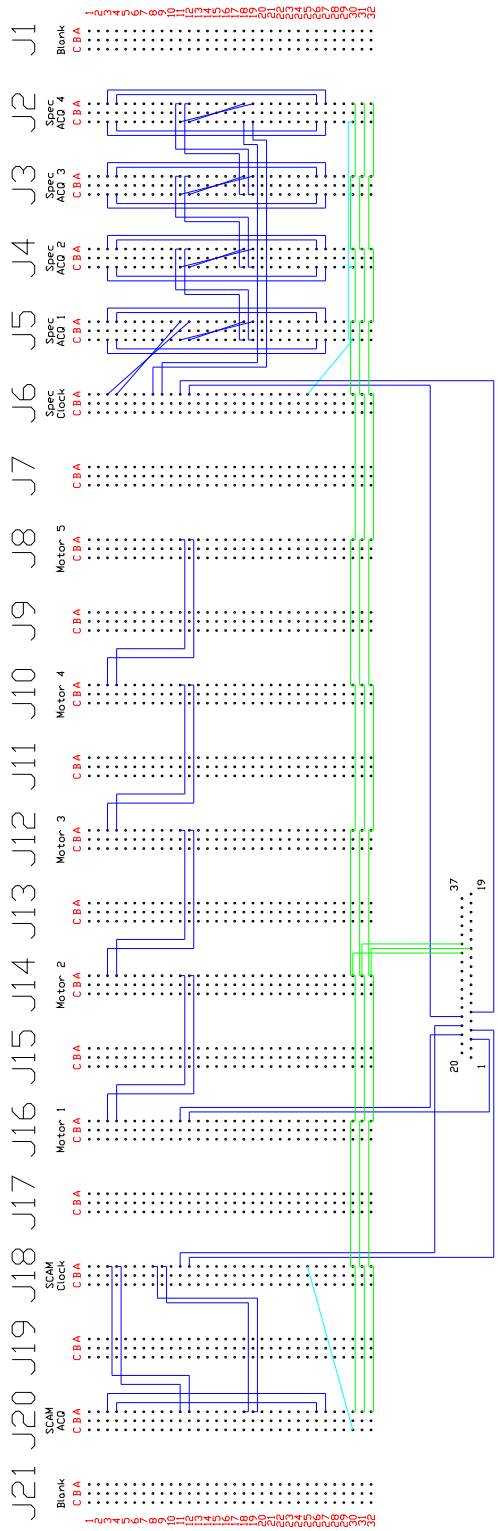

Figure 2: Backplane wiring

4 Connection lists

4.1 DB37 to backplane

	Connect	To	
Root out 0	DB37 - 3	J16 - A12	Motor 1 in 0
Root in 0	DB37 - 22	J16 - A11	Motor 1 out 0
Root out 1	DB37 - 4	J18 - A12	SCAM clock in 0
Root in 1	DB37 - 23	J18 - A11	SCAM clock out 0
Root out 2	DB37 - 24	J6 - A12	Spec. clock in 0
Root in 2	DB37 - 6	J6 - A11	Spec. clock out 0
NotReset0	DB37 - 31	J14 - A30	NotReset
NotAnalyse0	DB37 - 32	J14 - A31	NotAnalyse
NotError0	DB37 - 13	J14 - A32	NotError

4.2 Motor controller boards

	Connect	To	
Motor 1 out 1	J16 - A3	J14 - A12	Motor 2 in 0
Motor 1 in 1	J16 - A4	J14 - A11	Motor 2 out 0
Motor 2 out 1	J16 - A3	J14 - A12	Motor 3 in 0
Motor 2 in 1	J16 - A4	J14 - A11	Motor 3 out 0
Motor 3 out 1	J16 - A3	J14 - A12	Motor 4 in 0
Motor 3 in 1	J16 - A4	J14 - A11	Motor 4 out 0
Motor 4 out 1	J16 - A3	J14 - A12	Motor 5 in 0
Motor 4 in 1	J16 - A4	J14 - A11	Motor 5 out 0

4.3 Slit-viewing camera

	Connect	To	
Clock generator out 1	J18 - A3	J20 - A12	ACQ-A in 0
Clock generator in 1	J18 - A4	J20 - A11	ACQ-A out 0
ACQ-A out 1	J20 - A3	J20 - A27	ACQ-B in 0
ACQ-A in 1	J20 - A4	J20 - A26	ACQ-B out 0
ACQ-B out 1	J20 - A18	J18 - A9	Clock generator in 2
ACQ-B in 1B	J20 - A19	J18 - A8	Clock generator out 2

4.4 Spectrometer camera

	Connect	To	
Clock generator out 1	J6 - A3	J5 - A12	ACQ1-A in 0
Clock generator in 1	J6 - A4	J5 - A11	ACQ1-A out 0
ACQ1-A out 1	J5 - A3	J5 - A27	ACQ1-B in 0
ACQ1-A in 1	J5 - A4	J5 - A26	ACQ1-B out 0
ACQ1-B out 1	J5 - A18	J5 - C12	ACQ1-C in 0
ACQ1-B in 1	J5 - A19	J5 - C11	ACQ1-C out 0

ACQ1-C out 1	J5 - C3	J5 - C27	ACQ1-D in 0
ACQ1-C in 1	J5 - C4	J5 - C26	ACQ1-D out 0
ACQ1-D out 1	J5 - C18	J4 - A12	ACQ2-A in 0
ACQ1-D in 1	J5 - C19	J4 - A11	ACQ2-A out 0
ACQ2-A out 1	J4 - A3	J4 - A27	ACQ2-B in 0
ACQ2-A in 1	J4 - A4	J4 - A26	ACQ2-B out 0
ACQ2-B out 1	J4 - A18	J4 - C12	ACQ2-C in 0
ACQ2-B in 1	J4 - A19	J4 - C11	ACQ2-C out 0
ACQ2-C out 1	J4 - C3	J4 - C27	ACQ2-D in 0
ACQ2-C in 1	J4 - C4	J4 - C26	ACQ2-D out 0
ACQ2-D out 1	J4 - C18	J3 - A12	ACQ3-A in 0
ACQ2-D in 1	J4 - C19	J3 - A11	ACQ3-A out 0
ACQ3-A out 1	J3 - A3	J3 - A27	ACQ2-B in 0
ACQ3-A in 1	J3 - A4	J3 - A26	ACQ2-B out 0
ACQ3-B out 1	J3 - A18	J3 - C12	ACQ2-C in 0
ACQ3-B in 1	J3 - A19	J3 - C11	ACQ2-C out 0
ACQ3-C out 1	J3 - C3	J3 - C27	ACQ2-D in 0
ACQ3-C in 1	J3 - C4	J3 - C26	ACQ2-D out 0
ACQ3-D out 1	J3 - C18	J2 - A12	ACQ3-A in 0
ACQ3-D in 1	J3 - C19	J2 - A11	ACQ3-A out 0
ACQ4-A out 1	J2 - A3	J2 - A27	ACQ4-B in 0
ACQ4-A in 1	J2 - A4	J2 - A26	ACQ4-B out 0
ACQ4-B out 1	J2 - A18	J2 - C12	ACQ4-C in 0
ACQ4-B in 1	J2 - A19	J2 - C11	ACQ4-C out 0
ACQ4-C out 1	J2 - C3	J2 - C27	ACQ4-D in 0
ACQ4-C in 1	J2 - C4	J2 - C26	ACQ4-D out 0
ACQ4-D out 1	J2 - C18	J6 - A9	Clock generator in 2
ACQ4-D in 1	J2 - C19	J6 - A8	Clock generator out 2

4.5 Subsystem

	Connect	**To**
NotReset	J20 - A30	J18 - A30
	J18 - A30	J16 - A30
	J16 - A30	J14 - A30
	J14 - A30	J12 - A30
	J12 - A30	J10 - A30
	J10 - A30	J8 - A30
	J8 - A30	J6 - A30
	J6 - A30	J5 - A30
	J5 - A30	J4 - A30
	J4 - A30	J3 - A30
	J3 - A30	J2 - A30
NotAnalyse	J20 - A31	J18 - A31

	J18 - A31	J16 - A31
	J16 - A31	J14 - A31
	J14 - A31	J12 - A31
	J12 - A31	J10 - A31
	J10 - A31	J8 - A31
	J8 - A31	J6 - A31
	J6 - A31	J5 - A31
	J5 - A31	J4 - A31
	J4 - A31	J3 - A31
	J3 - A31	J2 - A31
NotError	J20 - A32	J18 - A32
	J18 - A32	J16 - A32
	J16 - A32	J14 - A32
	J14 - A32	J12 - A32
	J12 - A32	J10 - A32
	J10 - A32	J8 - A32
	J8 - A32	J6 - A32
	J6 - A32	J5 - A32
	J5 - A32	J4 - A32
	J4 - A32	J3 - A32
	J3 - A32	J2 - A32

4.6 Data read signals

	Connect	**To**	
SCAM			
Clock generator FIFORd out	J18 - A25	J20 - C30	ACQ FIFORd in
Spectrometer			
Clock generator FIFORd out	J6 - A25	J5 - C30	ACQ1 FIFORd in
ACQ1 FIFORd in	J5 - C30	J4 - C30	ACQ2 FIFORd in
ACQ2 FIFORd in	J4 - C30	J3 - C30	ACQ3 FIFORd in
ACQ3 FIFORd in	J3 - C30	J2 - C30	ACQ4 FIFORd in