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NIRSPEC

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NIRSPEC Electronics Design Note 15.01 - DAQ15 Description

Introduction

The DAQ15 is the NIRSPEC digital data acquisition board. Each DAQ15 board has four T805 transputers, running at 25 MHZ, with 4M of dynamic RAM per transputer. Each transputer has its own digital input port, 16 bits wide, feeding through a memory-mapped FIFO buffer 512 bytes deep. The FIFO buffers allow the transputers to read data asynchronously in blocks for co-adding and storage.

The DAQ15 was designed and built by DSP Systems, after extensive review of our proposed architecture, an evolution of that used in the Gemini twin-channel infrared camera.

System summary (see also NEDN01)

The Aladdin II 1024^2 infrared array has 32 analog outputs. These are fed as 16 pairs to 16 Preamp-A/D boards. Each Preamp-A/D board amplifies and filters the analog signals and digitizes them using two 16 bit A/Ds. Under the control of signals from the clock generator, the data from both A/Ds is multiplexed onto a single 16 bit output connector, which goes to the DAQ15.

Each DAQ15 board services 8 A/Ds (4 inputs times 2 A/Ds per input), so that NIRSPEC only needs four DAQ15 boards for the 1024^2 array. We use one more (actually only half of it) for the 256^2 slit-viewing camera array, which has 4 analog outputs.

Links

The hardware links between the four T805 transputers appear on the 96 pin DIN connector J2 at the rear of the board. The speeds of these links are selectable, link 0 on its own and the others as a group. The link speed for the whole board is controlled by a DIP switch, labeled S1, allowing 8 possible speed combinations. The speeds for each setting of S1 are listed below.

Link0	20MHz	20MHz	10MHz	10MHz	10MHz	10MHz	5MHz	5MHz
Link123	20MHz	10MHz	20MHz	10MHz	10MHz	5MHz	10MHz	5MHz
Switch 1A	off	off	off	off	on	on	on	on
Switch 1B	off	off	on	on	on	on	off	off
Switch 1C	off	on	off	on	on	off	on	off

Table 1 Link Speed Switch Settings

The DAQ15 has two 96 pin connectors (J1 and J2) at the rear of the board, allowing us to install it into a standard VME bus. These connectors draw power and ground from the VME backplane, but there is no connection from the board to any of the bussed VME signals, so if we were to plug a DAQ15 into a VME-based computer it would have no interaction with the rest of the system. However, the J2 connector of a VME bus has uncommitted pins on rows a and c, which we use to make our transputer link connections, using wire-wraps. The pinouts are given below. The last letter of each link name tells you which of the 4 CPUs (a, b, c, d) it connects.

	J2A	**J2C**
1	ground	ground
2	unused	unused
3	LinkOut1a	LinkOut1c
4	LinkIn1a	LinkIn1c
5	ground	ground
6	ground	ground
7	unused	unused
8	LinkOut2a	LinkOut2c
9	LinkIn2a	LinkIn2c
10	ground	ground
11	LinkOut0a	LinkOut0c
12	LinkIn0a	LinkIn0c
13	LinkOut3a	LinkOut3c
14	LinkIn3a	LinkIn3c
15	unused	unused
16	ground	ground
17	unused	unused
18	LinkOut1b	LinkOut1d
19	LinkIn1b	LinkIn1d
20	ground	ground
21	ground	ground
22	unused	unused
23	LinkOut2b	LinkOut2d
24	LinkIn2b	LinkIn2d
25	ground	ground
26	LinkOut0b	LinkOut0d
27	LinkIn0b	LinkIn0d
28	LinkOut3b	LinkOut3d
29	LinkIn3b	LinkIn3d
30	notSubReset	Sync1In
31	notSubAnaylse	Sync2in
32	notSubError	spareInt

Table 2 DIN-96 Link pinouts (note that they are incorrect in the original documents).

The four Transputers on the DAQ15 can be easily identified. Transputer A is U1 and is on the left side of the board when the DIN connectors are on the edge away from the viewer (or at the top when plugged into the VME bus). Transputer D is U4 and is on the right hand side. Transputer B is U2 and Transputer C is U3.

DAQ15 Inputs

The DAQ15 has four high density DB-26 female connectors. Each connector feeds the 16 bit data from a Preamp-A/D board into a 16 bit wide, 512 word deep FIFO composed of two 8 bit Cypress 7201 512 word FIFOs. Each 16 bit wide FIFO is controlled by a single Transputer. The double nature of the FIFO is transparent to the user - it appears as a single object.

A Field Programmable Gate Array (FPGA) between the FIFOs and the controlling transputer maps the FIFO data into the transputer's memory space. Data can be read from fixed memory addresses in various formats. The FPGA logic also provides interrupt and status bits to the transputer so that the transputer can monitor the state of the FIFO, such as Not Empty, Half Full or Full. The transputer can also empty the FIFO to clear unwanted data, such as before an observation or after one has been aborted.

Important Note: The DAQ15s do not directly control the flow of data from the A/Ds! The board requires an external **write** signal in order to write data into the FIFO. Similarly, the A/D boards must receive external signals telling the A/Ds to **convert**, and a **select** signal which controls which A/D's output is fed to the output connector. The DAQ17 Clock/Motor board provides the **write**, **convert** and **select** clocks, so the whole data taking sequence is determined by the clock waveforms it produces.

The DAQ15 is fully isolated from the A/D board. The DB-26 connector also provides the +5 volts and ground required by the DAQ15 side of the ISO150 isolators on the Preamp-A/D boards.

1 ground	14 D10
2 D2	15 D13
3 D5	16 ground
4 D8	17 ground
5 D11	18 +5
6 D14	19 D0
7 ground	20 D3
8 +5	21 D6
9 +5	22 D9
10 ground	23 D12
11 D1	24 D15
12 D4	25 FifoClk
13 D7	26 10k resistor to ground, unnassigned

Table 3 Fifo Connector Pinouts

Note that D0 is the *least significant bit* (LSB) of the A/D data and D15 is the most significant bit (MSB). The 16 bit A/D converter data sheet defines D15 as the LSB and D0 as the MSB. This has been corrected in the A/D board layout so that D0 on the DB-26 connector on the A/D board is the LSB, matching what the DAQ15 (and the rest of the world) expects to see. This is only significant if directly probing at the data coming out of the A/Ds.

Other Inputs

Each Transputer monitors its FIFO Half Full and Not Empty flag bits, but the FIFO's input must be clocked externally. This is done via the backplane. The DAQ15 expects to see a FIFO clock on either of the Sync pins on the backplane. The Sync pulses come from the controlling DAQ17 and should really be called FIFO Write or FIFO Clock pulses. The Sync inputs are described on page 18 of the DAQ15 schematics. The DIN 96 pinouts are on page 1 of the schematics (note that DSP Systems only included schematic pages 1,10 and 18 (of 19)). Sync1 is on J2C-30, Sync2 is on J2C-31 and Spare is on J2C-32.

The DAQ15 board allows a wide variety of FIFO clock sources and clocking permutations, depending on the number of Sync clocks (one or two) and the jumpers on the routing header blocks. Header blocks JP5, JP6, JP7 and JP8 (see Sch. pg 18) control the routing of the Sync pulses to the four FIFOs. For example, if Sync1 is selected as the Fifo Clock signal, then all the header blocks should have a jumper between pins 1 & 2. The Sync pulse is then buffered and relabeled FifoClkA through FifoClkD. For simplicity, NIRSPEC currently uses a single FIFO clock on Sync1, so the header routing blocks should be jumpered as described.

The external FIFO clock can also be provided via the DB-26 connector for each FIFO. The connector has the option of providing an external FifoClk signal for its related FIFO. This option is controlled by header blocks JP1 through JP4. The current NIRSPEC design does not provide for a Preamp-A/D board generated FIFO clock, so these header blocks must have jumpers between pins 2 & 3. This passes the buffered FiFoClk signal from the backplane to the FIFO.

The DAQ15 has several diagnostic LEDs that can be controlled via software, by writing to fixed addresses. The controlling circuitry is included in the missing schematic pages, so I don't know exactly what makes them work. These are mostly useful for software diagnostics. As of this writing we have not brought the LEDs out to the front panels. It is unlikely we will do so.