NIRSPEC

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NIRSPEC Electronics Design Note 10.00
Operation of the Aladdin 1024 x 1024 Detector

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The purpose of this note is to provide a brief summary of what is currently known about the operation of the Aladdin 1024 x 1024 InSb array from SBRC, in order to assist in specifiying the NIRSPEC Infrared Electronics system.

1. Basic Characteristics

For completeness and reference, the published specifications for the Hughes-SBRC 1024 × 1024 InSb array (Aladdin) are summarized in Table 1.

Table I Characteristics of Aladdin Array

IR material	Thinned InSb photodiodes
	Reverse-biassed diodes
Format	1024(H) x 1024(V)
Pixels	1,048,576
Size	27 μm square
Fill Factor	100%
Architecture	512 x 512 quadrants
Readout	CMOS shift registers
	PMOS SFD unit cell
	PMOS (or NMOS) output drivers
Outputs	32; 8 per quadrant
Frame Rate	50 ms; 20 Hz max
Reset	By rows or global only
	Destructive or non-destructive
Full well	300,000 electrons at 0.8 V bias
Wavelength	0.9 - 5.3 μm
	AR coating peaked at H band
Temperature	35 K (typical)
Dark current	< 0.1 e/s/pixel @ 0.4 V bias
Noise	< 25 e rms
QE	> 80% (1 - 5 μm)
Bad pixels	<0.5%
	No bad rows or columns

So far, no problems have been found with the new readout device. Only one run has been carried out so it is difficult to gauge yield figures; certainly no better than 1 out of 10. Column bus level control appears to have eliminated the "charge-dumping" effect which reduced the useful bias across the detector in the 256x256 array. Noise is not as good as above specification (1 device tested) and operability on the tested device was ~90%, not 99.5%. See Al Fowler's paper in Appendix A2.

The Aladdin array has four independent quadrants which are "mirror images" of each other and appear as shown in Figure 1. The first pixel of each quadrant is always in the outer corner and the last pixel is always in the center (inner corner of a quadrant).

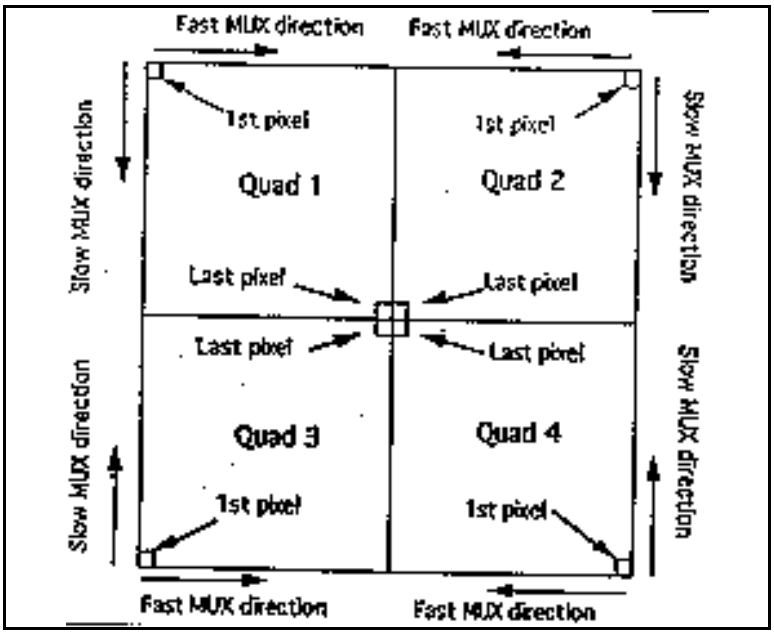

Figure 1 Layout of the Aladdin array as 4 quadrants.

Each output reads every 8th column in its quadrant. For example, consider quadrant No.3 (bottom left). The fast or "column" register reads left to right in this quadrant. The first pixel read out is the outside corner pixel which appears on Ouptut 1. The next pixel read out is the next one to the right on the same row, but its signal appears on Output 2. It is not until the 9th pixel in that row that another signal appears on Output 1. There are therefore only 64 output signals from a given output per row (8 x 64 = 512).

There is a chamfer at 45° across one of the corners of the chip carrier which identifies pins 1 and 124. If the chamfer is at the top left as the chip is viewed from above, then Pin 1 is at the top left and pin numbers increase down the left side to Pin 31, along the bottom left to right from 32 - 62, up the right hand side from 63 - 93, and along the top from right to left are pins 94 - 124. See Appendix A1 for complete list of pins.

Clocks and unit cell bias levels are contained along the left and right sides from pins 1 - 31 and 63 - 93. Output, output cell bias levels and a diagnostic pulse - Tend, are on the lower and upper edges from pins 32 - 62 and 94 - 124. Pins 1 and 31, and pins 63 and 93 are all Vggcl. Similarly, pins 2, 30, 64, 92 are all Vddcl and so on. Pin 16 and Pin 78 are unique and this is Vsub. Pin 47 and Pin 109 are also unique as the mid-points of the top and bottom rows; these pins are Vdetcom.

Each quadrant is electrically isolated except for Vsub (ground) and Vdetcom.

2. CLOCK SUMMARY

All 8 clocks work with a 6 volt swing from 0.0 V to -6.0 V. There are no positive voltages and there are no voltages more negative than -6 V. Clocks are buffered on the chip. Also, because the Aladdin array has CMOS shift registers, the clocks are "edge-triggered" and fast (<< 1μs) and without any shaping.

Phi S Sync	Starts slow (row) shift register: 0 to -6 V
Phi S1, Phi S2, Phi S3	3 phase clocking of slow shift register: 512 row positions. "Make-before-break" concept.
Phi F Sync	Starts fast (column) shift register.
Phi F1, Phi F2	2 phase clocking of fast shift register: 64 column positions. "Break-before-make" as in the current 256x256 array.
Phi RST	Resets detector bias (1 row or all rows). Pulses a transfer gate. Actual reset levels determined by filtered bias lines.

3. BIAS SUMMARY

Most of the bias voltages are dc levels between 0.0 Volts and -6.0 Volts. A few of the bias levels need to be "switchable" to different levels for optimum operation, but are NOT clocks in the normal sense. The dc level applied usually holds for at least a frame readout time or for the integration time.

Vdetcom	Detector common supply	-3.0 V
Vdduc	Drain for column line and unit cell	-3.5 V
	Current 0.6 mA normal, 6mA peak	
	Detector Bias = (Vdetcom - Vdduc) = 0.5 V	
Vssuc	Source for column line	0.0 V
Vddcl	Clamp for column line	
	Switchable	-1.4, -3.5 V
Vggcl	Clamps column lines to Vddcl	
	Switchable	-4.9, -2.7 V
Vddout	Output drain supply (8 -16 mA)	
	Low, to reduce glow	-1.0 to -1.3 V
Vref (Vslew,Vidle)	Supply for Iref (Islew, Iidle)	
	Requires 125 kΩ resistor to ...	-1.8 to -2.0 V
Vrston	Unit cell reset gate in ON position	-5.6 V

Vrstoff	Unit cell reset gate in OFF position For GLOBAL RESET set Vrstoff = Vrston RC filter shaping required; τ = 1 - 2 μs	-2.0 V
Vrowon	Unit cell Row Enable gate in ON position	-5.6 V
Vrowoff	Unit cell Row Enable gate, OFF position	-0.7 V
Vpcol, Vprow	High supply for shift registers	-0.5 to 0.0 V
Vncol	Low supply for column shift register	-3.5 V
Vnrow	Low supply for row shift register	-5.6 V

Note that a few values which could be 0.0 V or -6.0 V have been "tweaked" to values like -0.5, -0.7 or -5.6, -3.5 V. Some of this is done to reduce power dissipation and glow. All of the bias voltages should be heavily filtered and very low noise. Alan Hoffman suggests that the high current bias lines should have a decoupling capacitor e.g. between Vdduc and Vssuc, between Vncol and Vpcol, Vnrow and Vprow. He did not give a value and I don't think Al Fowler does this; probably 0.1 μF or smaller.

There are also 8 outputs per quadrant. Each requires an external load. The outputs are in the -1 V to 0.0 V range typically, with a 0.5 V swing for a 500 mV reverse bias; the outputs are essentially the same as the 256x256 chip. A 10 kΩ resistor to ground would give about 100 μA. Alternatively, a 100 μA constant current source should be used; Al Fowler says he always uses a constant current source. The total capacitance load on the output due to coax etc. should be less than 50 pF to maintain the 20 Hz frame rate. I am not sure what kind of cabling he uses, only that he keeps the length as short as possible.

Finally, there is 1 diagnostic output per quadrant (Tend) which senses the end of row and column shift registers; it requires a 10 kΩ load.

4. DETECTOR RESET

The Unit Cell is a 3-transistor design instead of the 4-transistor approach used in the 256x256 chip. As a consequence, you can no longer reset pixel by pixel. You can reset a row at a time or you can perform a GLOBAL reset. The latter is possible because the reset "enable" function is controlled by a transfer gate; the reset off level (Vrstoff) is switched to the Vrston level.

There are three things associated with the reset function. Two heavily-filtered, very stable voltages Vrston (-5.6 V) and Vrstoff (-2.0 V), and a reset clock pulse PhiRST (0 to -6.0 V). Typically, one would feed a Harris HS201 switch with these two voltages. The HS201 output is fed through two RC filters to set the rise and fall times to around 1 - 2 μs before sending these voltages to the chip. When you want to use the global reset option you must send a digital pulse to the Harris switch to make the Vrstoff line change value and then return to its normal value. The required new value is simply the Vrston voltage. A shaped pulse is produced which ensures uniformity of reset.

You can also reset a row by addressing the row and switching Vrstoff between its normal value and Vrston to get a shaped pulse reset of that row. If switching of the HS201 is NOT employed, then reset is done by the PhiRST clock in conjunction with the row shift register enable to switch the transfer gate on the chip to perform a reset on that row.

5. CLOCKING SEQUENCE FOR A QUADRANT

1. Start the slow (row) shift register. Phi S Sync pulses from 0 V to -6.0 V and back; same for ALL clocks below. Pulse widths of about 1 μs are OK.

Pulse PhiS1. Negative edge turns on Row 1.
Pulse Phi S2. Negative edge turns off Row 0 in this "make-before-break" action.
Row 1 is now enabled.

2. Start the fast (column) shift register. Phi F Sync pulses from 0 V to -6.0 V and back.

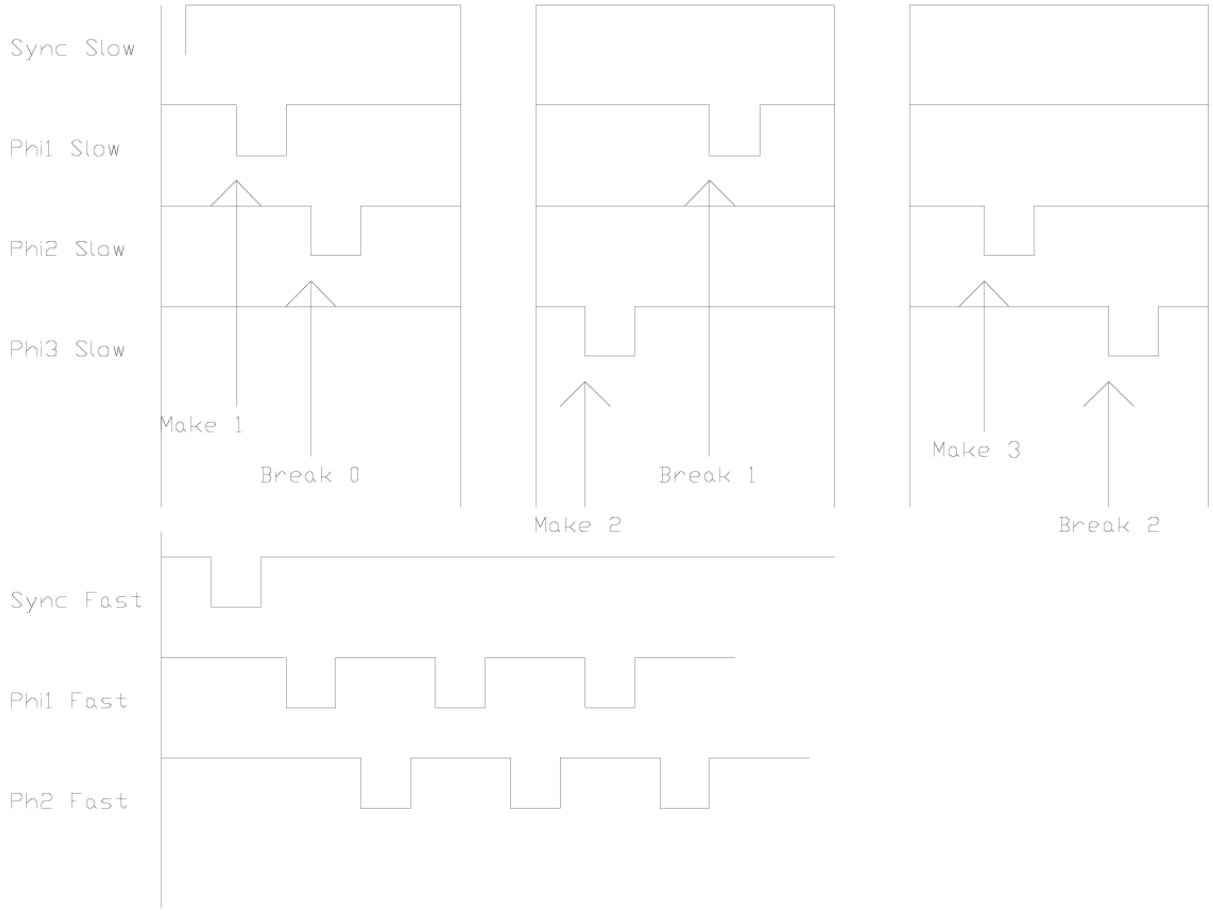

Figure 2 Slow and fast clock sequence illustrating "make-before-break" action of the 3-phase row (slow) clock. Note that our clocks are buffered on the chip and used to "edge-trigger" a shift register.

3. Clock the fast register through 64 columns. Send stream of 0 V to -6.0 V pulses on PhiF1 and PhiF2. Start with PhiF1. Pulse width = 1.3 μs, delay 0.1 μs and send PhiF2 with pulse width of 1.3 μs also. Delay 0.1 μs and send PhiF1 again. Fast clocks repeat every 2.8 μs. Each negative edge addresses the next column in a "break-before-make" action.

4. Clock the slow register by one row.

Pulse PhiS3 (next in sequence). Negative edge turns on (makes) row 2.
Pulse PhiS1 (next in sequence). Negative edge turns off (breaks) row 1.
Row 2 is now enabled.

5. Repeat steps 2 through 4, 512 times total

For Row 3, pulse PhiS2 and then PhiS3 (next in sequence)
For Row 4, pulse PhiS1 and then PhiS2
For Row 5, pulse PhiS3 and then PhiS1
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For Row 511, pulse PhiS1 and then PhiS2
For Row 512, pulse PhiS3 and then PhiS1
For Row 513, pulse PhiS2 and then PhiS3. This action "makes" an imaginary connection and "breaks" the real conncetion to 512; otherwise it would remain addressed.

Could group the "slow" sequence in a pattern of 171 repeats.

6. Questions and Answers about 1024^2 array operation

1. Q. Do the optimum bias and clock voltage levels vary from those published by SBRC?
A. Yes. In general, SBRC use values of either 0 or -6 V. Al Fowler "tweaks" these to reduce power dissipation, glow, unnecessary voltage swings etc.; the values given here are from Al Fowler.

2. Q. Do any bias voltages need stepping?
A. Yes. Al Fowlers currently switches Vggcl, Vddcl, Vrstoff between two well-filtered, dc voltage settings. These are not clocks, and the switching should occur on the bias board. The

new voltage is generally in place for at least a frame time. I recommend designing for four switchable bias lines.

3. Q. Are all the clocks square waves or do they need RC shaping?
A. All clocks are square waves and should have fast rise and fall times. Clocks are buffered on the chip and negative-going edges are used to trigger the CMOS shift register.
The bias voltages Vrston, Vrstoff should be fed through a Harris switch and then each should pass through RC filter circuits to control the rise and fall time of the pulse which is effectively produced by activating the Harris switch to set the Vrstoff level to the Vrston level for a few microseconds. The rise and fall time should be 1 - 2 μs.

4. Q. What is the impedance of the output FETs at 35 K?
A. Answers vary. SBRC gives 700 Ω, Al Fowler (NOAO) gives 1 kΩ.

5. Q. Do the outputs require a current source?
A. It is not essential, but Al Fowler always uses one. Current should be about 100 μA. Can also use a 10 kΩ resistor to ground (output voltage - 1 volt). Al Fowler uses a 2N4393 or some such part - not absolutely sure.

6. Q. What is typical output voltage range and offset?
A. Same as the 256x256 array. Typically, -1.5 V to -0.5 V for a 1 volt swing for a large well depth. In practice, I think our well depth will be < 0.5 V, so about -1.5 V to -1.0 V.

7. Q. Are Zener diodes required for static protection?
A. As I understand it, there is some protection on the chip. Al Fowler does not use Zeners in his set up, but Alan Hoffman of SBRC recommends 10 V Zener diodes on ALL pins!

8. Q. What are the current requirements?
A. The clocks are buffered, so the current requirement transfers to the power supplpy lines to the chip. Some bias lines (drains) can draw several mA. As far as I could tell, the peak load was about 16 mA.

9. Q. Are any of the inputs more noise-sensitive than others?
A. No, but the reset levels (Vrston, Vrstoff) and the clamp levels (Vggcl, Vddcl) should be heavily filtered and very quiet to get the best effect. Otherwise, probably the same as the 256x256 chip. The best noise achieved so far with 16 samples in Fowler sampling mode - 20 electrons rms. With only one sample the noise is about 40 electrons at a bandwidth of 60 kHz and 80 electrons at 1.2 MHz.

10. Q. What is the maximum readout rate?
A. Quoted as 20 Hz (50 ms frame time)

11. Q. Is the Aladdin array sensitive to "latch-up"?

A. Not known. No adverse experiences so far.

12. Q. How severe are the quadrant to quadrant and column to column variations in the output transistors? Can a single offset adjustment be used for all preamps?
A. Column to column fix-pattern effects seen in the 256x256 devices has been reduced in the Aladdin chips by using "current mirrors" to give control and uniformity of the unit cell drain current. For stability, a minimum current (**Iidle**) flows in each column at all times. Using a "look-ahead" design, the column being read *and* the next column both have a higher current (**Islew**) flowing during readout. This gives fast response and minimizes power dissipation. I think it should be OK to use a single offset.