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NIRSPEC Electronics Design Note 08.00
Selectable Gain and Bandwidth Circuits

1. INTRODUCTION

To optimized the system performances to the particular target type, an adjustable gain and bandwidth circuits are best, where the gain and bandwidth could be optimized for best signal-to-noise and resolution. For best resolution, the gain should be set to the highest possible without causing the target signal to be saturated. And for best signal-to-noise, the bandwidth should be limited to the smallest bandwidth required for given scan rate. By reducing the bandwidth, the noise will be reduced by square root of the bandwidth reduction and signal will remain the same; therefore, the signal-to-noise will be increased.

The minimum bandwidth required is directly related to the settling time and scan rate. The settling time is defined as time for step response to settle to within specified accuracy of the steady-state value. It is a function of the scan rate, CCD set-up time and A/D aperture time. For a step input, the settling time (t_s) for an ±½ bit out 16 bits (±0.000763%) can be expressed as follows:

$$t_s(\pm 0.000763\%) = t_{\text{scan rate}} - t_{\text{CCD set-up}} - t_{\text{A/D aperture time}}$$

where $t_{\text{scan rate}}=1/f_{\text{scan}}$; $t_{\text{CCD set-up}}$. 4µsec; $t_{\text{A/D aperture time}}$ = 200 nsec

The relationship between the bandwidth (f_{-3db}) and t_s for a 2nd order Bessel low pass filter to an accuracy of ±0.000763%, is as follows:

$$t_s=1.7946/f_{-3db}$$

A capacitor digital isolator, ISO150, will be used to isolate the four address bits from the critical analog circuit. Two of the address bits are for gain selections and other two are for the bandwidth selections, as shows in Figure 1. This isolator will reduce the noises from pickup or ground loop. All the digital selection components follow the isolator will be filtered and slow down as required to reduce any crosstalk or noise pickup to the analog path. Since, the switches and decoder are not switching in normal operating mode. Both devices could be treated as an analog device.

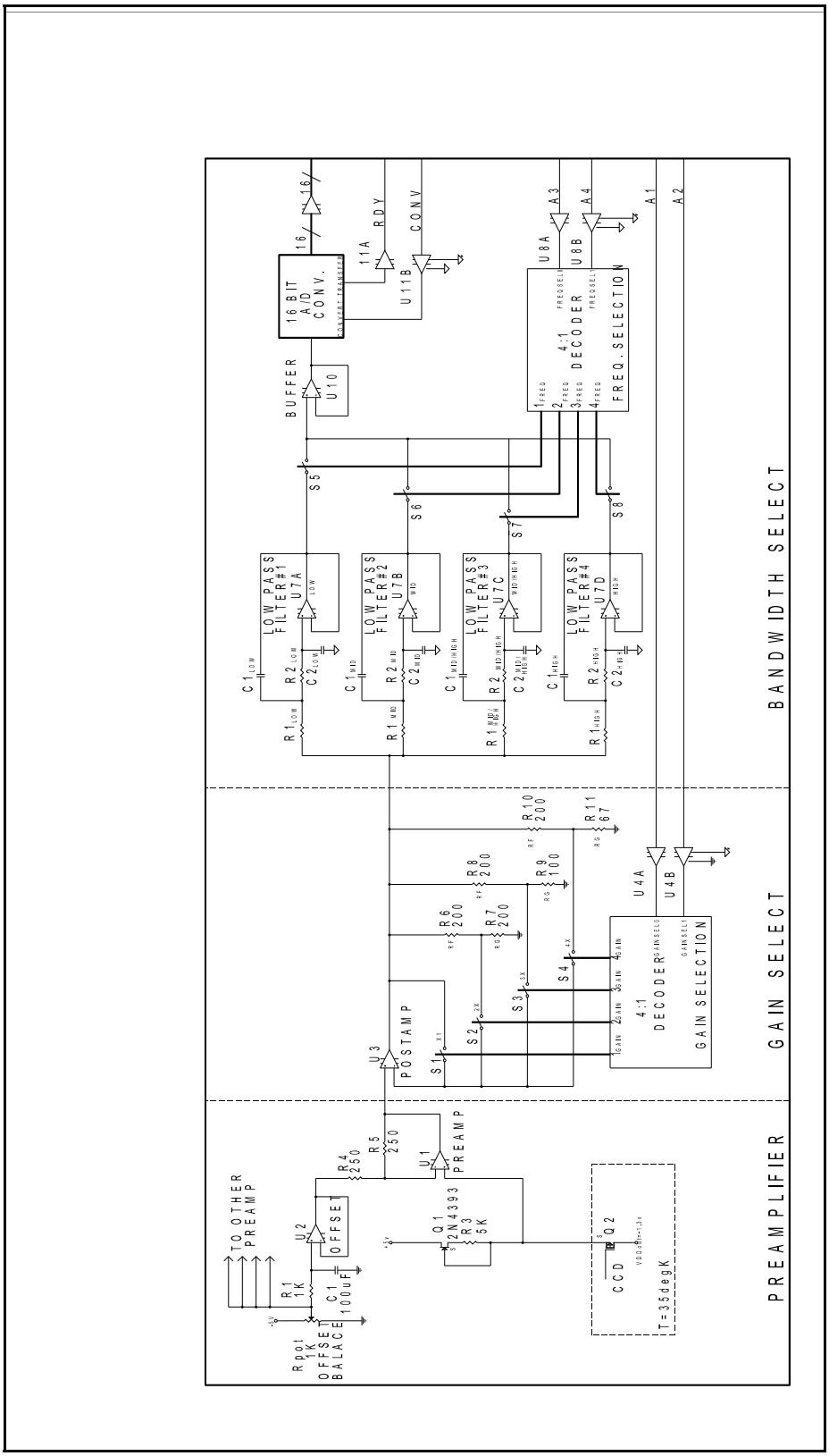

Figure 1 Analog Signal Processsor Circuit

2. SELECTABLE GAIN CIRCUIT

The optimum location for the Selectable Gain circuit is after the preamplifier, as shown in Figure 1. This will maximized the signal level before the A/D board located on different electronic box. With the higher signal, the susceptibility to pickup will be greatly reduced. Figure 2 shows the Selectable Gain circuit. The 1:4 decoder will select one of the four gain settings according to the two gain address bits (A1 and A2).

The gain will be one, when S1 is on. The gain will be $+(1+R_6/R_7)$, when S2 is on. Similar for S3 and S4, the gain will be set by the corresponding pair of resistors (R_F,R_G). The gain is $A_v=+(1+R_F/R_G)$. All gain setting will be non-inverting and equal to one or higher.

Since the switches (S1..S4) are connected to high impedance node of the opamp (U3), and inside the high gain feedback loop as shown in Figure 2, the signal distortion due to the variation of the switch's r_{on} will be negligible.

Due to the switch's capacitance on the summing node, the noise gain will be increased as shown in Figure 3. The noise will increase linearly starting at corner frequency of $f_2=1/\{2\pi R_G C_G\}$. For a typical quad switch, total capacitance at summing junction is 62 pF. And taken the worst case when R_G = 200 ohm, the noise gain will increase starting at 12.8 MHz, as shown in Figure 3b. The high frequency noise gain can be reduced by adding a feedback capacitor, C_F, as shown in Figure 2. The capacitance C_F will act as 1st order low pass filter with the bandwidth of $f_1=1/\{2\pi R_F C_F\}$. Also, C_F will serve to stabilize the opamp from oscillating due to added capacitance C_G. However, the bandwidth of low pass filter f_1 must be set higher than required bandwidth for the system. A graph of gain vs frequency, showing the effect of C_G and C_F is shown on Figure 3.

Since, the summing junction of opamp (U3) is very sensitive to any capacitance coupling, special precaution must be taken during board layout to reduce the length and location of this track. And the added gain switches will increase complexity of the printed circuit board.

As a conclusion, with proper precaution taken as mention above, this Gain Selection circuit will operate satisfactorily if system bandwidth requirement is less than 1 MHz.

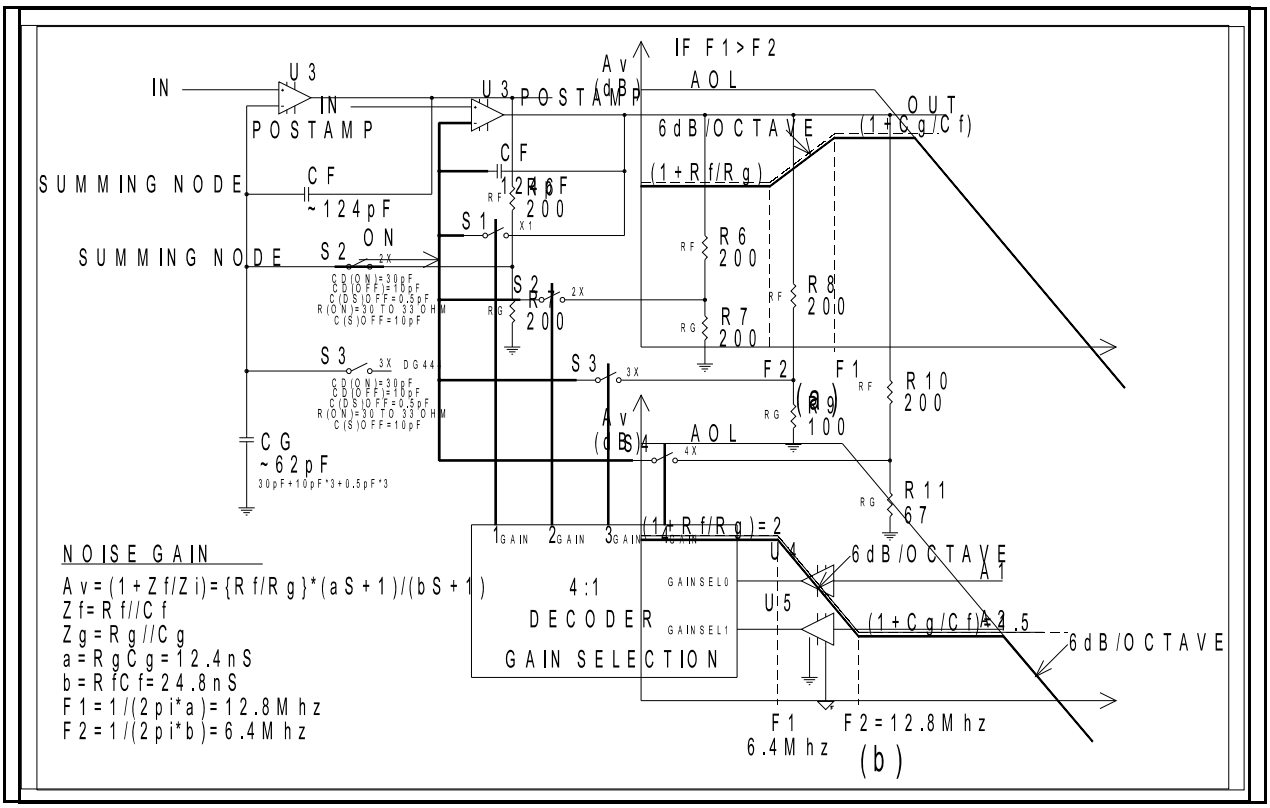

Figure 32 Noise Select Circuit Frequency Response - Gain Circuit

3. SELCTABLE FREQUENCY CIRCUIT

The Selectable Frequency circuit is best place after the instrumentation amplifier and before the A/D converter, as shown in Figure 1. The low pass filter will remove any unwanted pickup and noise above the bandwidth of the system requirement before going into A/D converter. Due to scan readout rate can change from 2 Khz to 400 Khz. The frequency bandwidth should change proportionally to reduce the unnecessary bandwidth which in turns, reduces the total noise level to Analog to Digital converter.

Figure 4 shows the Selectable Frequency circuit. The frequency bandwidth is selected by two address bits (A3 and A4). The one out four decoder will select one of the four bandwidth circuits.

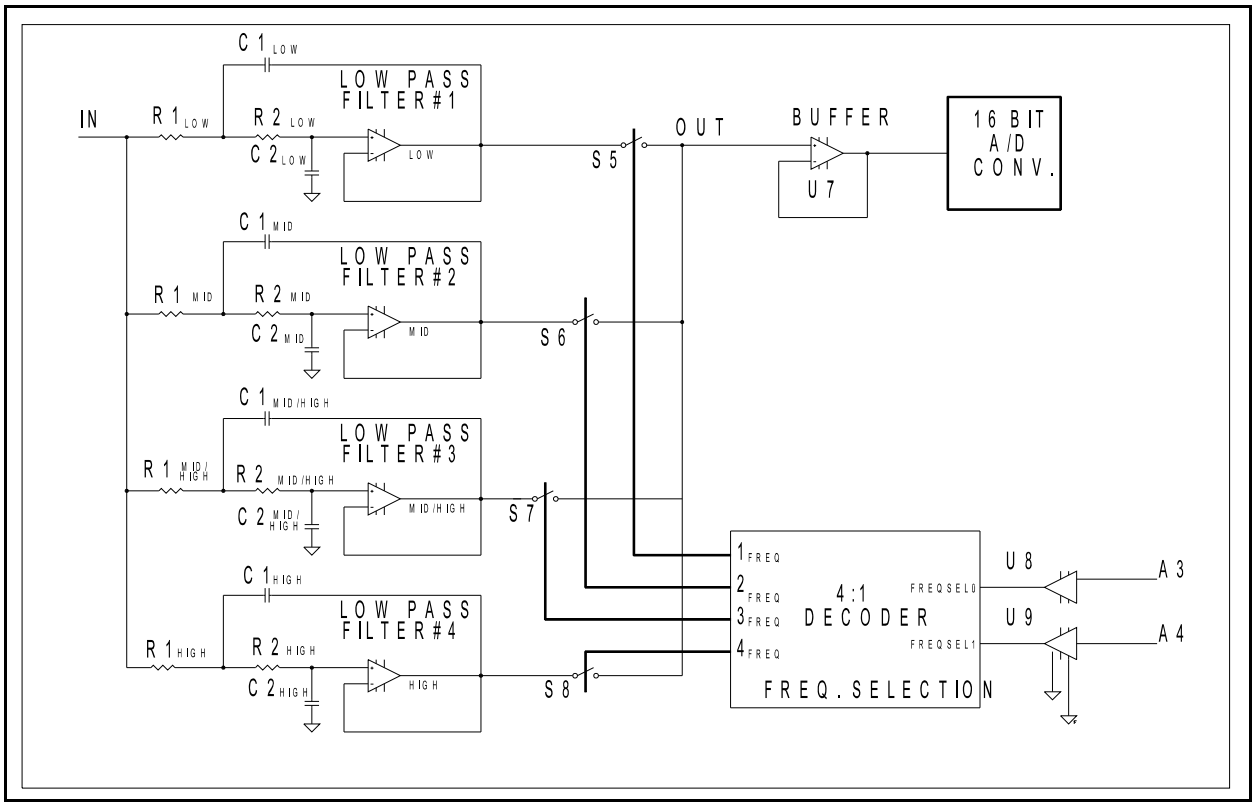

Figure 4 Bandwidth Select Circuit

It is much better to have four different independent bandwidth circuits, one for each bandwidth. Because a solid state switch has a finite resistor value and changes with voltage level and temperature, it will be difficult to control the frequency bandwidth and roll-off characteristic accuracy.

The commonly used "3-dB" signal bandwidth (f_{-3dB}) of an amplifier is defined as the frequency of the half-power point. The half-power point is value on the frequency axis where the signal has been reduced by 3dB from the reference value. A 3-db reduction represents a loss of 50% in power level and corresponds to a voltage level equal to 1/%& of the voltage at the reference. Figure 4 shows a unity gain low pass filter called Sallen-Key. The frequency response for any 2nd order unity gain low pass filter can be expressed as shown in Equation 1. The relationship between

the f_{-3dB} point and natural frequency f_o, can be solved by solving equation 1 for f_{-3dB}. The natural frequency f_o and damping factor ζ, as function of circuit component values, are given by Equation 1 below:

$$A_v(s) = \frac{f_o^2}{s^2 + 2\zeta f_o s + f_o^2} \Rightarrow |A_v(f_{-3db})| = \left| \frac{f_o^2}{(f_o^2 - f_{-3dB}^2) + j2\zeta f_o^2 f_{-3dB}^2} \right| = \frac{1}{\sqrt{2}}$$

$$where\ \zeta = \frac{1}{2Q} = \frac{R1 + R2}{2}\sqrt{\frac{C_2}{R_1 R_2 C_1}}; \quad f_o = \frac{1}{2\pi\sqrt{R_1 C_1 R_2 C_2}}$$

Equation 1 General 2nd Order Low Pass Filter

The damping factor (ζ) and "f_{-3dB} vs f_o" for Bessel low pass filter are defined as follows:

$$\zeta \equiv \frac{\sqrt{3}}{2} = 0.866 \ ; \ f_{-3dB} = \sqrt{\frac{-1+\sqrt{5}}{2}} f_o = 0.786 f_o$$

Equation 2 Bessel Low Pass Filter

The solid-state switches (S1 ... S4) have no effect on the Bessel filter because it is not in the filter circuit. There will be no distortion or gain changes due to changes in r_{on} because the signal is buffered with a high impedance amplifier, U7.