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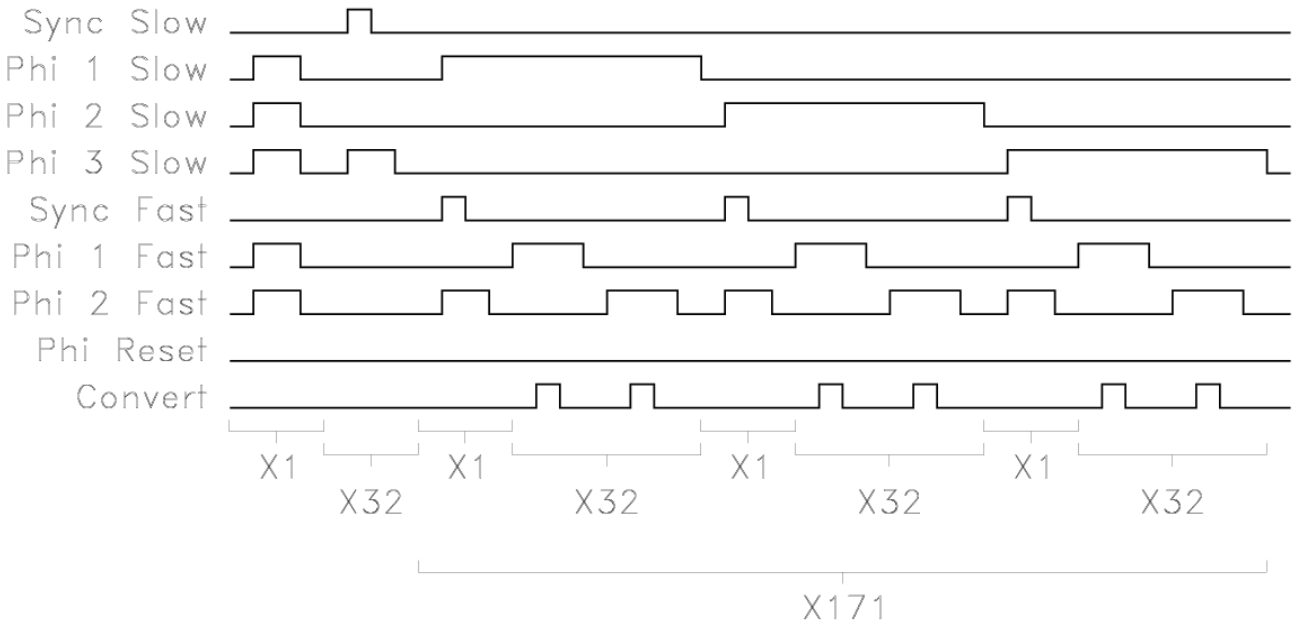
NIRSPEC Electronics Design Note 04.01 - SBRC 1024^2 Array Clocking

Introduction

In order to design our clock generator and level shifter we need to understand the requirements of the new SBRC 1024^2 array. From a conversation with Alan Hoffman and from looking at the document supplied to us by Al Fowler, I have been trying to figure out what the clocking waveforms are. The main differences between this array and the 256^2 are that there are three phases to the slow clock rather than two, and the array is organized as 512^2 quadrants.

Below I have plotted a timing diagram which I think shows how to clock through the array once, reading each pixel. It may be there are some details wrong, but I will send this note to Alan Hoffman and ask him to verify that it is correct, or in what way it is wrong.



The way I have drawn the waveform, it is as close as it could be to the way we clock the 256^2 array. The function of each segment is described below.

a First of all, each shift register has to be reset by turning on all of its clock phases together. If we have just successfully clocked the array all the way through, this step should not be necessary, since each register will have "finished", and be in reset state, but there is no harm putting in this short sequence to be sure. This sequence is performed once.

b Next we need to load a pulse into the slow register, effectively at row 0, where row 1 is the first real row. To do this we turn on the Sync and one of the phases at the same time. In the 256^2 device it is Sync and Phi 2, and here I used Phi 3. I am not clear on which should go high first or which should go low first. This sequence is performed once.

c Now we want to be on row 1, so we raise Phi 1 Slow (and leave it on to the end of the row). To start off on the 0th column of the array, we turn on the Sync and Phi 2 of the fast clock register, just as on the 256^2. This is done once, at the beginning of the row.

d In this segment we clock through the pixels along the row, by alternately making first Phi 1 Fast and Phi 2 Fast high. Each time we clock either phase, we select eight pixels in each quadrant to be output. Repeating this segment 32 times outputs 8 * 2 * 32 = 512 pixels, the whole row in each quadrant.

e As **c**, except now we drop Phi 1 Slow and raise Phi 2.

f As **d**.

g As **c**, except now we drop Phi 2 Slow and raise Phi 3.

h As **d**.

Once we have gone through steps **c** to **h** we have done one set of three rows. We have to repeat this at least 171 times to do the full 512 rows, although since 171 times 3 is 513 I am not exactly sure how to deal with the last row.