NIRSPEC

UCLA Astrophysics Program **U.C. Berkeley** **W.M.Keck Observatory**

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NIRSPEC Electronics Design Note 02.03
Transputer boards

1 Introduction

Although the transputer boards designed some years ago for the Gemini system perform very well, we saw a need for improved designs in order to meet the more stringent requirements of NIRSPEC. After a number of iterations and discussions with DSP Systems, we came up with this set of specifications for the custom transputer boards required for NIRSPEC.

For a full understanding of the system, this document should be read in conjunction with the latest versions of NEDN01, which describes the overall architecture, and NEDN11, which discusses the physical packaging and interconnections.

2 Clock generator/motor controller boards

2.1 Overall description

The overall architecture of these boards is shown in Figure 1 below. The boards were designed to have two separate functions, clock generation and motor control. These functions were performed by separate boards in the Gemini system, but since those boards were so similar architecturally, we decided to combine the functionality in one layout for NIRSPEC. We plan to have several copies of this board (including a spare). Two will be used as clock generators and at least two as motor controllers, although they will all be completely populated with all functions on board, so as to be interchangeable with each other and the spare.

Clock output is a parallel data stream passed through a FIFO (First-In-First-Out) buffer. The clock waveforms required to drive the detector arrays are very repetitive, so the transputer software generates a subsection of the waveform and feeds it to the FIFO. To send out the complete waveform the transputer loads a repeat count into a register, then sets a control bit to turn on the FIFO output clock. Once the first copy of the sub-waveform is sent out, the FIFO re-transmit feature is used to repeat the sequence the number of times defined by the repeat count. Since the FIFO output is controlled by a hardware clock, the timing of the output is completely stable and repeatable.

Short sections of the waveform at start and end are not repeated. In order to send these out just once, a second clock output facility is provided via a memory-mapped port known as the “bypass” port. Data written to this port appear on the same physical output as the FIFO output.

Motor control output is via a set of simple memory-mapped parallel ports. The transputer software generates the motor control pulses by writing directly to the output addresses of these ports. For each motor the transputer generates step pulses and a direction signal, plus control bits for power on/off or high/low power. These pulses and control signals are sent to commercial driver modules which produce the multiple phases at appropriate currents to drive the motors. After some discussion of the number and placement of front panel connectors, it was agreed that there will be four motor ports per board.

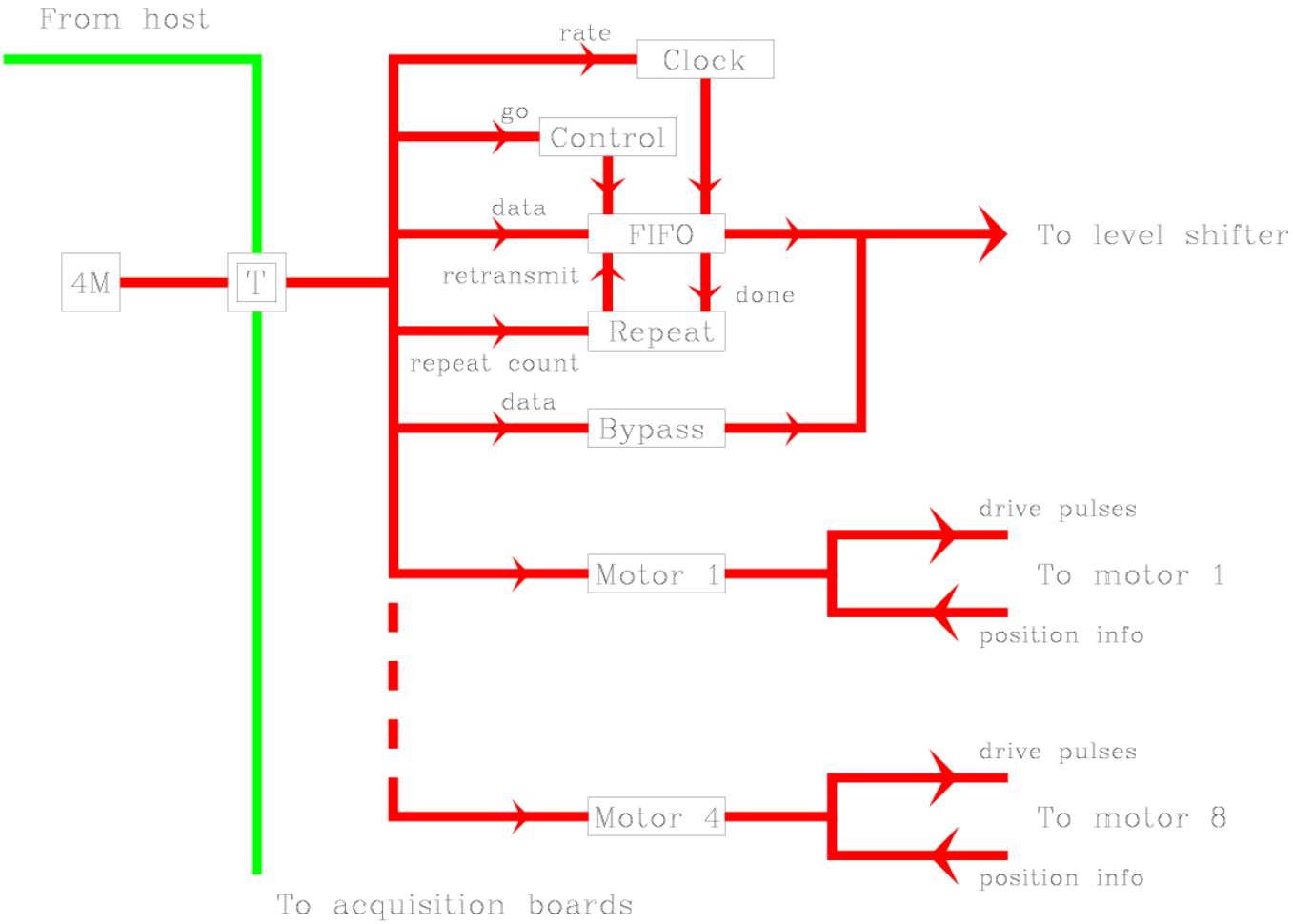

Figure 1: Clock board architecture

The matching memory-mapped input ports are used to read in status input (usually from microswitches) from the mechanisms. Interpretation of these switch inputs is specific to each mechanism and is handled by the transputer code.

2.2 Number of clock output bits

The spectrometer camera section of NIRSPEC will use the SBRC "Aladdin" 1024^2 device, which requires one more clock line than the 256^2 array. We will also need other clock lines for a number of different functions, so our first step was to count up the potential requirements.

Clocking the 1024^2 array requires nine lines including the convert pulse. We have to clock (albeit slowly) some lines which are nominally DC biases in order to optimize the performance of the arrays. These will probably number at least two. We will need one line to control multiplexing of two A-Ds into a single buffer on the acquisition boards. We will also need four lines to control switchable analog gain and analog filter bandwidth.

This means we will probably have to provide a *minimum* of 16 lines, compared to the nine available on the Gemini board. Since the word size of the transputer is 32 bits, we will go all the way to 32 bits. This will allow plenty of lines for expansion, and also make the board more general purpose.

2.3 Clock output rate

The A-D we will most likely use (Analogic ADC4325) can be operated at 500 kHz maximum, though we will usually run it slower. The waveforms for clocking arrays typically require about 10 time slices between A-D convert pulses, implying the minimum time slice would need to be 200 ns. The Gemini boards needed a 50 ns time slice to drive the 256^2 array at up to 2 MHZ, so this is easily achievable.

A new feature of this board design, and an improvement over the Gemini boards, is a programmable FIFO output rate. In order to change the frame rate, we need to either pad out the waveform data (by repeating some of the output words many times), or slow down the clock rate driving the FIFO output. If we have a simple way to change the clock rate from software it makes the programmer's job simpler, and more importantly avoids the problem of overflowing the FIFO output buffer with an overly extended waveform.

2.4 FIFO size

The Gemini clock boards started out with 4k deep FIFOs, and were upgraded to 16k later when we started pushing the limits of the 4k size with complex multiple sampling waveforms. The waveforms for clocking the 1024^2 array are not yet entirely clear, but it looks like they will be pretty similar in complexity to those for the 256^2 devices. The 1024^2 array is organized as four 512^2 quadrants which we will operate in sync, so the amount of data required to clock each line will be roughly twice as long as for the 256^2 array. There are three phases to the slow clock rather than two, so we will have to load the waveform to drive three lines rather than two into the FIFO, so as to have our minimum repeatable sub-waveform. Overall this means we will need roughly three times as much FIFO capacity as for the 256^2 devices, so the 16k FIFO size should be adequate. There are also

larger FIFOs in the works from the manufacturers, but in any case having the switchable output rate will allow us to avoid padding of the waveform and so will cut down the waveform size quite a bit.

2.5 Isolation

In the new system we intend to do everything possible to reduce noise. One aspect of this effort is that we will completely isolate the digital and analog sections of the system. To achieve this we will use the ISO150 isolator chip from Burr-Brown. We have seen some noise reduction by using an add-on board using this device between the clock generator and level shifter in the Gemini system. Since the level shifter will probably have the more stringent space constraints, we will put the isolator chips on the output side of the clock generator board.

2.6 Memory

The Gemini clock generator boards have 1 megabyte of DRAM, and despite our efforts to optimize the program, we have found memory space to be a limitation at times. The memory chips used in the Gemini design have also become harder to obtain as manufacturers have switched production to larger sizes. We will have 4 megabytes of RAM on the new design.

2.7 Motor control feature

The number of motors we will need to drive is not yet fixed, but may be as many as eight. We will organize the motor output as four memory-mapped ports with 8 bits of I/O on each. We will need to use several copies of the motor controller board to handle all the motors. We will probably never use as many as 8 bits of output on a single port, but there may be a requirement for a fair number of input bits to provide complete redundancy of positional information for some of the mechanisms.

The motor control ports could also be used in the boards used as clock generators to control the switchable gain and bandwidth of the analog section, and also to control and monitor other components of the system, such as housekeeping electronics.

3 Data acquisition boards

3.1 Overall description

The acquisition boards are required to read in 16-bit parallel data from the A-D converters, and when necessary co-add successive frames in memory until sufficient signal-to-noise has built up in the accumulated image. Data input is through FIFO buffers to the four transputers on each board.

There are 32 analog output channels on the 1024^2 array, and one A-D converter per analog channel. We decided not to multiplex the analog signals to cut down the number of A-Ds, since there would be a noise penalty. We will however multiplex the digital data so that two A-Ds feed their data to each transputer input port.

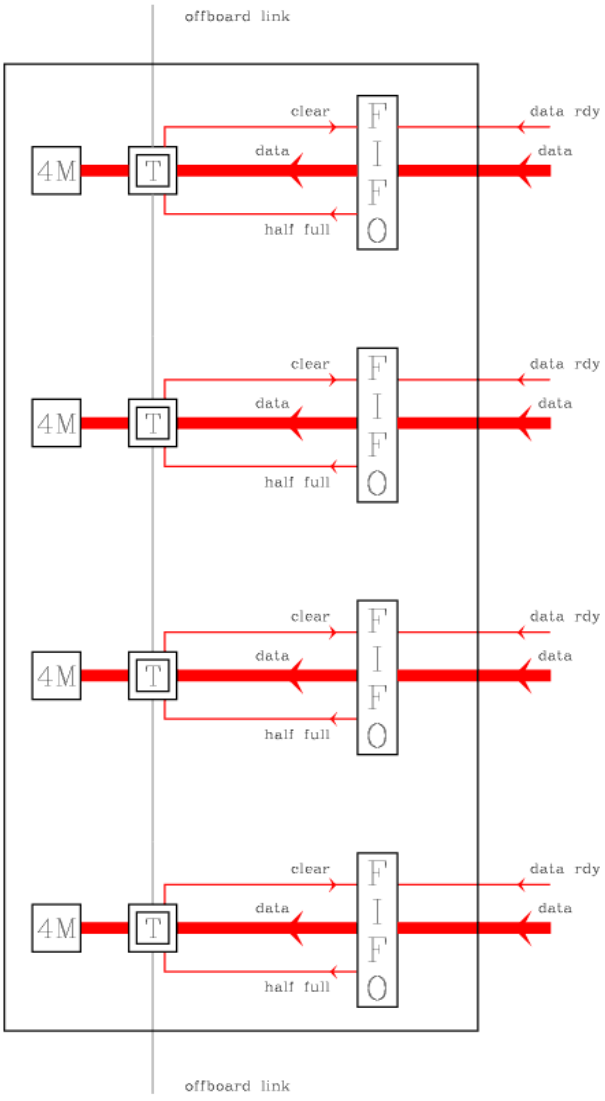

Figure 2: Acquisition board architecture

3.2 A-D interface

In NIRSPEC we are aiming for an extremely low noise system, the target being <±½ bit for a 16 bit A-D. We have found that the DAQ13 boards used in Gemini are limited in their noise performance by crosstalk between digital and analog sections, so in this design we will separate the A-Ds completely from the acquisition system. The A-Ds will be on separate boards, housed in their own cardcage with their own power supply. As with the clock generator and motor control system, we will use ISO150 isolator chips, so that there will be no common ground between the A-D and the FIFO buffers feeding the data to the transputers. The acquisition boards then become fairly generic parallel input boards, reading in 16-bit data from any external device whenever they get a data ready signal. The architecture of the boards is shown to the left in Figure 2.

The data ready signal will come from the clock generator board, which will also control the multiplexing of the two A-D outputs onto the ribbon cable. This keeps both the transputer and A-D boards simpler, and increases flexibility. A consequence of this arrangement is that unlike the more tightly coupled Gemini

system, we will not have the whole system hang up because one A-D converter goes out. We will simply get bad data from that channel but the rest of the array intact. This may or may not be a virtue, since we will have no way of knowing that an A-D has gone out or is not functioning properly until we examine the data. Some further work ir required to come up with the best solution to this problem.

3.3 Performance

We have done calculations of the worst-case flux onto the detector, which sets the speed requirement for the system as being able to read in and co-add the whole array in approximately a third of a second. Rounding up to the next power of two, we will design for four frames per second. That means we require 4 million pixels per second of co-adding speed to single-sample the array. We know from our early benchmark tests for the Gemini system that this requirement can be met by four T805-25 transputers. To do double correlated sampling will require a minimum of eight processors.

The current layout agreed with DSP Systems will actually give us 16 transputers reading from the 32 A-D converters, so there is no problem meeting the speed requirement. Cutting down the number of processing transputers any further would require that we spend more of each pixel time multiplexing the data from the converters and passing it to the transputers, since in order to minimize crosstalk we must read all the data off the A-D boards before digitizing the next set of pixels.

3.4 Programming interface

One of the main reasons we are sticking with transputers for this system is the inheritability of the software from the Gemini system. Therefore we need the programming interface to be just the same, although it wouldn't matter if a few addresses were to change. The interface will be a little simpler than the Gemini system with the A-D converters not being on the same boards.

4 Off the shelf boards

We need some off the shelf components in addition to the two custom board designs described in the preceding sections. These have to perform the functions of host to transputer interface, long-distance communication and control and monitoring of temperature sensors and controllers.

4.1 Host to transputer connection

I looked into a number of options for this role. We could have chosen either a card plugged into the Sun workstation's internal Sbus, or a product from Transtech called the Matchbox. Support software for use with the Solaris operating system (Sun's version of Unix) is only available for the Matchbox, which eliminates the other option. The Matchbox is a SCSI-2 interface board packaged

in a case with power supply, and connected to the external SCSI port of the workstation. Firmware on the board and support software in the Sun allow the transputer on the Matchbox board to be the root transputer of a transputer network. The Matchbox costs $3500 from Transtech, less a 30% educational discount.

An issue I had to resolve was the question of whether to have a separate enclosure for the TRAM module used for the long distance connection (see next section). One options was to buy a Transtech TTM50 SCSI-2 TRAM, which is essentially the same as the board used in the Matchbox. If specified to have the proper firmware it is functionally identical to the Matchbox. Thus the SCSI-2 connection and the communications TRAM could be combined in one enclosure, on a TRAM motherboard. However since we are mostly in a design phase, I decided we should just buy the standard Matchbox, in order that we can get started right away with software prototyping and testing, without having to buy a case, power supply and TRAM motherboard and build up the system that way. At a later date we can investigate the possibility of combining the boards in one enclosure.

An advantage of using the Matchbox is that it is not confined to one type of workstation, or to one individual workstation (so it could be switched to another computer quickly in event of a problem). One caveat is that software for the Matchbox is only supported on a subset of the Unix implementations available today. Solaris is fine so we will have no problem if we don't switch from the Sparcstation/Solaris combination to some unusual machine.

4.2 Long-distance connection

The long distance connection between the root transputer and the rest of the network needs to cover approximately 300 feet, and provide reliable noise-immune transmission. On Gemini we have used differential TRAMs which appear to work well, but there is some question of whether they provide complete isolation between the host PC ground and the front end system ground. For the NIRSPEC system it seems a good idea to use a fiber-optic connection, since the electrical environment of the telescope dome is pretty noisy. This can be implemented using off the shelf TRAMs available through DSP Systems, from a UK company called Sundance. A pair of TRAMS gives us one 20 Mbits/s transputer link plus the "subsystem" signals required to operate the remote network. This connection can be up to 1 kilometer in length. They use an industry standard type of fiber-optic cable, which we will have to specify to the CARA engineers for installation in the Keck II cable wraps.

4.3 Temperature control and monitoring

The device we will most likely use for temperature control and monitoring are LakeShore units similar to the ones we use on the Gemini camera. These have an RS232 connection and a very simple programming interface. We did consider putting RS232 capability on the combined clock generator/motor controller boards, but decided this was too complicated. We will use a commercial RS232 TRAM module instead.

5 Miscellaneous details

Through our discussions with DSP Systems there were a number of details we worked out such as physical connections. This section lists those agreed points, so that they are clearly stated. The list is taken from a series of FAXes sent during the month of August 1995. There was a confusion over numbering hence the section 3a below.

1. The clock output signals to the level shifter board, offset board and bias board will be isolated using Burr-Brown ISO150 devices, located on the UCLA supplied boards.

2. The clock generator/motor controller board will supply power to drive the external ISO150 devices.

3. The clock/motor board design is to have 4 rather than eight motor ports. Each port will have 8bit output and 8 bit input capability, plus 5V power and ground.

3a. The motor output ports have DB25 female connectors. DSP Systems to select brand and layout, but probably best to use 2 double stacking connectors. Pinouts flexible since the I/O is to/from flexible transputer code.

4. Estimated cable length between clock/motor board and motor driver modules is 18" - 24".

5. Motor driver inputs require 6-15mA per bit. Drivers on motor ports will be socketed allowing a range of drive capabilities. For motor drive modules an open collector driver will be used.

6. The motor controller ports will reset to low.

7. The motor controller ports will have a watchdog timer, selected on a port by port basis. This will prevent motors being powered up for excessive periods after a move is over. Normal program operation will always turn off motor power after completion of a move, but if this doesn't happen for any reason, the timer will shut down the motors and set the transputer error bit.

8. DSP Systems will try to add bidirectional capability to one port of the clock/motor controller board for use with temperature sensor chips.

9. The clock port output clock will be programmable. Clock output rates will be derived from a fixed frequency oscillator (40 MHZ) and a programmable divider, giving output frequencies in the range of 5 MHZ and below. For further flexibility, the oscillator will be socketed.

10. Three lines of the clock output will be split off to give Convert, Select and Latch signals. The Convert and Select signals will come out on BNC connectors and go to the offset board where they will be isolated. The Latch signal will go to an uncommitted pin on the VME P2 connector, and from there to the DAQ boards in the same crate.

11. The processors on each clock/motor controller board will be a 30 MHZ T805 transputer with 4 MBytes DRAM if possible, or at least a T805-25 part.

12. The transputer links will be routed to the P2 VME connector according to DSP Systems' standard link pin assignments.

13. The clock board will provide the Latch signal which will be used to clock data into the input FIFO buffer. This signal will be active high.

14. The clock output connector will be a DB50 female in a DB37 size shell (3 rows of pins). This may require that not all signal conductors will be interleaved with ground conductors.

15. The data input connector will be a DB37 female connector, for which the pinassignments are given below.

16. DSP Systems will provide comprehensive documentation for the supplied boards along with test transputer code to be used to verify proper operation.

PREAMPLIFIER/ADC P3 CONNECTOR

P3-1	DO0		
		P3-20	GND
P3-2	D01		
		P3-21	GND
P3-3	DO2		
		P3-22	GND
P3-4	DO3		
		P3-23	GND
P3-5	DO4		
		P3-24	GND
P3-6	DO5		
		P3-25	GND
P3-7	DO6		
		P3-26	GND
P3-8	D07		
		P3-27	GND
P3-9	DO8		
		P3-28	GND
P3-10	DO9		
		P3-29	GND
P3-11	DO10		
		P3-30	GND
P3-12	DO11		
		P3-31	GND
P3-13	DO12		
		P3-32	GND
P3-14	DO13		
		P3-33	GND
P3-15	DO14		
		P3-34	GND
P3-16	D015		
		P3-35	GND
P3-17	+5V*		
		P3-36	GND
P3-18	+5V*		
		P3-37	GND
P3-19	spare