

1.3 Noise

Very low noise performance is absolutely essential. The goal is $\pm 1/2$ bit with a 16-bit A-D, or 6 electrons rms. This is about an order of magnitude better than we achieve with Gemini, but given that we will be running much slower it should be achievable. There are other design documents dealing with the analog design. The main architectural improvement is the removal of the A-D converters from the acquisition boards to minimize crosstalk, using isolator chips to completely separate the analog and digital sections.

1.4 Communication

We need to transfer data and commands between the Sun host and the front end system over long distances (about 300 feet) without errors, at an adequate speed. We need to decide on a figure for what we consider adequate speed, but I will do an end to end analysis later in this document, highlighting where the limiting bottleneck in the system will occur.

1.5 Motion control

The system must be able to control stepper motor based mechanisms both inside and close to the dewar. If possible we want to use the same format as in the Gemini system, where the motor controller provides step pulses plus direction and power on/off signals to the power driver modules. As in Gemini we also need to read back several bits of datum switch information for each mechanism.

1.6 Feedback of status

Information on instrument status (e.g. temperature, mechanism position) must be read back to the to the host computer for display of status and notification of problems.

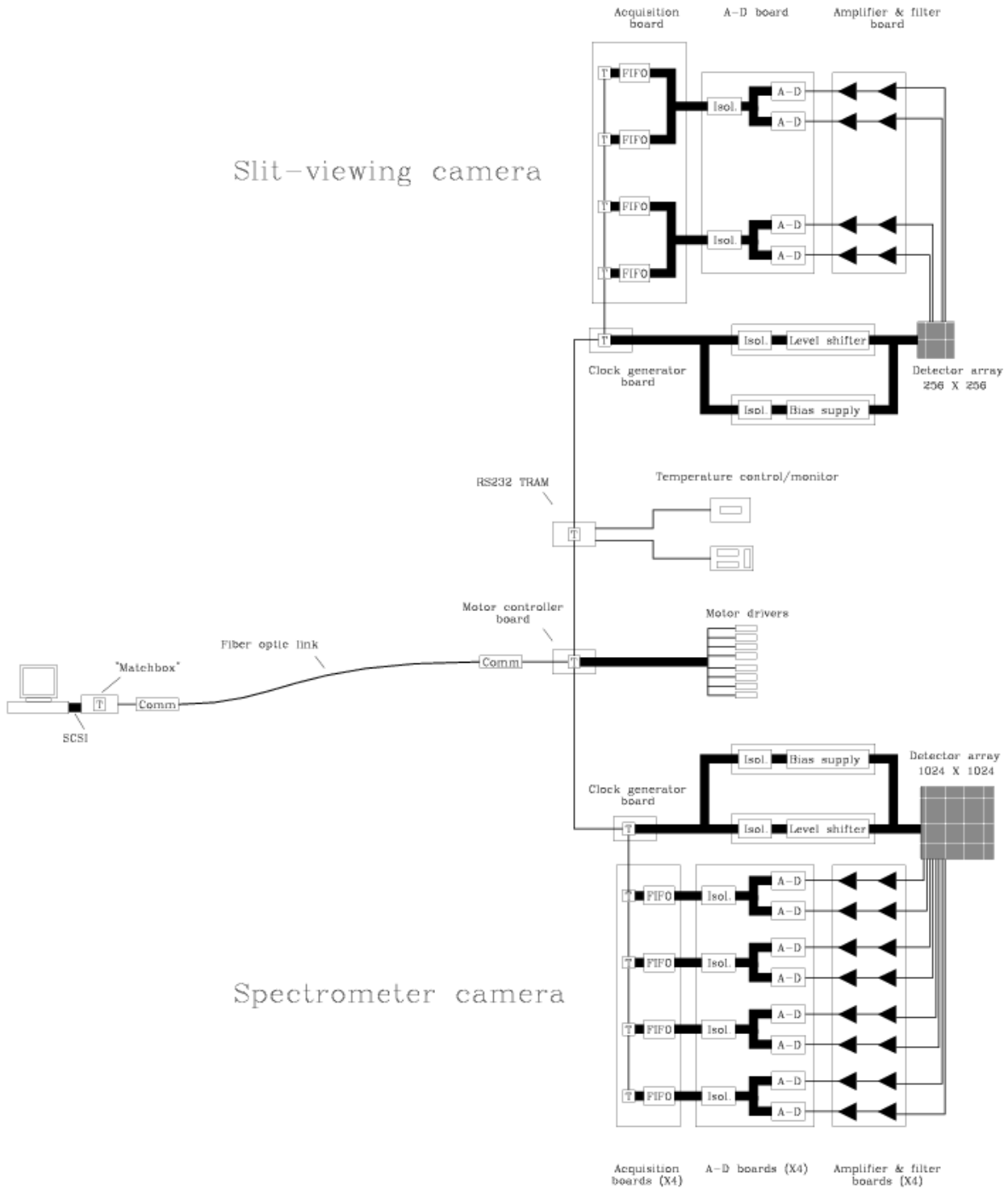
1.7 Packaging

The system must be compact, rugged and easy to maintain in the field. Everything needs to be modular with spares for all boards provided. There are a number of constraints such as provision of cooling to prevent perturbations to dome seeing, the necessity of keeping the analog electronics close to the detectors, and making sure everything is adequately shielded against outside interference.

2 Overall architecture

2.1 Description

The current conception of the architecture of the system is shown in Figure 1 below.



This architecture is very similar to the Gemini system already in use, with a number of improvements, and a different host computer (Sparc 10). As with the Gemini system, most of the transputers are located close to the instrument, communicating over a long distance with the "root" transputer connected directly to the host. In this case the host-transputer link uses a Transtech Matchbox interface unit which attaches to the external SCSI port of the Sparcstation. The long distance link will be fiber-optic to give both isolation and noise immunity.

In order to improve noise performance the A-Ds are on separate cards, isolated from the transputer acquisition cards using Burr-Brown ISO150 isolator chips. The clock generator boards are similarly isolated from the level shifters. There will be no common ground or power supply between the analog electronics and the digital electronics, which will be housed in completely separate enclosures with separate power supplies.

The custom transputer boards required for this version of the system are a new clock generator board, very similar to the Gemini one but with the addition of general purpose I/O for use as a motor controller, and new acquisition boards similar to the Gemini DAQ13 boards but without the A-Ds and post-amps. There is one acquisition transputer for every two A-D converters, since a 1:1 ratio would mean we would have far too many transputers (see processing speed discussion below). For a full description of the format of each board see NEDN 2.01.

2.2 Does it meet the goals?

The architecture was developed to meet all of the goals outlined in section 1. I will go through them all in turn.

2.2.1 Clocking

The design has both the required speed and an adequate number of clock lines (32). The addition of a programmable clock rate will also make the programming of different timings easier to achieve.

2.2.2 Processing speed

The stated requirement was for the system to read in and co-add the whole array in approximately a third of a second. Rounding up to the next power of two gives four frames per second. That means we require 4 megapixels/second co-adding speed to single-sample the array, which can be met by four T805-25 transputers. To do double correlated sampling will require a minimum of eight processors.

The current proposal from DSP Systems would actually give us 16 transputers to read from the 32 A-D converters, so there is no problem meeting the speed requirement, but is this overkill? Cutting down the number of processing transputers any further would require that we spend more of each pixel time multiplexing the data from the converters and passing it to the transputers, since in order to minimize crosstalk we must read all the data off the board before digitizing the next set

of pixels. Obviously multiplexing 4:1 would also make our A-D boards a little more complicated. This issue needs to be explored further before a final specification for the boards is agreed with DSP Systems.

2.2.3 Noise

We have done all we can to isolate the analog and digital sections. The only possible drawback now is that the transputers are still in the same neighborhood as the analog section. We must pay careful attention to packaging issues, such as using shielded enclosure for the card cages to cut down on cross-talk.

2.2.4 Communications

The communication between the host Sparcstation and the transputer network will be via the external SCSI port of the workstation to a Transtech product called the Matchbox. There will be some software overhead in developing the communication protocol between the Sparcstation and the transputer in the Matchbox, but as in the Gemini system we can base this protocol on the "iserver" program supplied as part of the transputer development system.

From the Matchbox we will go to a pair of fiber-optic TRAM modules, providing a transparent link from the host system to the front end enclosure. Communication using these fiber-optic TRAMS will be error-free due to the transputer-transputer error-correcting protocol built into the transputer hardware.

The fiber-optic link will give us just over 800 kilobytes/second over the 300 feet or so we will be driving it. This translates to around 5 seconds to transfer a 1024^2 frame (4 bytes per co-added pixel). After an exposure time of several minutes (or even tens of minutes) this does not represent a great loss of observing efficiency.

If we want to pull 256^2 frames back from the slit-viewing camera quickly, such as when the observer is peaking up the target object on the slit, we might forego the co-adding, so we could achieve about 6 frames per second (2 bytes per pixel). When taking co-added data frames in the normal observing mode, we would be able to transfer at half that frame rate.

2.2.5 Motion control

The motion control facilities will be essentially the same as the Gemini controller except for additional lines of switch/status input, giving us enough channels and enough bits of I/O to handle all of the mechanisms we are proposing so far.

2.2.6 Feedback

Status information from the instrument mechanisms can be interpreted and fed back from the motor controller transputer. Additional feedback from serial interface devices such as temperature monitors will be dealt with using an off the shelf RS232 TRAM. This solution is simpler than the alternative idea of adding RS232 capability to the clock generator/motor controller hybrid design.

2.2.7 Packaging

Although we are satisfied with most aspects of the performance of the Gemini transputer boards, we have had problems with the packaging. The main problem is that we can't easily remove one board without removing the whole front panel assembly of the front end electronics box. Part of the problem lies with our own design of the front panel, which we had to create because the boards themselves lack individual front panels.

What we would like to do this time is settle on a standard board size, 6U Eurocard, and make everything in that size, with a front panel on each board. Thus any board could be removed at any time without having to undo more than the screws holding it in place and any external cables connected to it. Given the added motor control functions we are adding to the clock generator boards, additional edge connector space would be needed anyway, forcing it up to that size from 3U. If space on the boards becomes a problem there is no particular need to stick with the standard 160 mm depth of standard VME boards. We could accommodate 220 mm boards (like the Gemini DAQ13 boards) if necessary in off-the-shelf card cages.

The packaging of the transputer system will be fairly compact, given that there will only nine 6U VME format boards involved. These will comprise four acquisition boards for the 1024^2 array, one for the 256^2 array, two clock generator boards, one motor controller board and a TRAM motherboard for the fiber-optic and RS232 TRAMs. We will also need a TRAM motherboard in the crate next to the Matchbox for the matching fiber-optic TRAM.

The analog electronics will probably occupy a similar volume. We will use the same form factor (6U Eurocard) for all boards, with the probable exception of the analog amplifiers. These need to be placed as close as possible to the detectors, so they may be squeezed into some form factor which accommodates this requirement.

3 Discussion and conclusions

The main points in favor of this architecture are its relative simplicity, the fact that it requires only two new transputer board layouts, and its inheritance from the Gemini system. The logical layout is the same as the Gemini system, and although physically the clock generator and motor controller have been laid out on the same PCB design, each section works pretty much as before. The acquisition boards are simplified by the removal of the A-Ds and post-amplifiers, but should have a very similar programming interface.

We are still left with the transputers in close proximity to the analog electronics. However the correct grounding scheme, separation of power supplies, use of isolators etc. should protect against cross-talk from digital to analog sections having any unfavorable influence on the final result. It is worth noting that although the NOAO "Wildfire" system removes the co-adding transputers from close proximity to the instrument, they still have their clock generator transputer right next to their dewar.

The only drawback I can see is that the use of a single fiber-optic link may be a bottleneck in the overall data transfer throughput of the system. However even if the data were to arrive faster at the host end transputer, the system would then be bottlenecked at the SCSI interface into the Sparcstation, at around 1 MByte/s. This later figure should become firmer when the Matchbox system is delivered in a few weeks, and we can run some benchmark tests with our own prototype software.