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NIRSPEC Electronics Application Note 13.00

Transputer network and backplane wiring

1 Introduction

The NIRSPEC transputer boards[1] plug into a standard VME backplane. The backplane is not used as a VME bus in the normal way; rather it's used as a convenient way to provide power and ground to the boards. We can also use standard hardware (connectors, card cages etc.) in the 19" form factor. Another advantage of using VME is that the VME backplane has a lot of uncommitted pins on the P2 connector. The transputer links and subsystem signals are brought out to these uncommitted pins, where we can link them up as we need to, using wirewraps for permanent connections, and jumper cables for temporary links. This note describes the physical layout of the transputer network, and all of the interconnections on the backplane.

2 Transputer network description

The host computer (a Sparcstation) interfaces to the transputer system using a unit called a MatchBox, made by Transtech. The MatchBox interfaces to the external SCSI port of the host computer. Coupled with the Transtech driver software, the Matchbox gives us a single transputer serial link to the front end transputers. It is important to note that transputer links are *not* RS232, RS422 or any other standard that can be used over long distances. They are TTL level signals, only reliable over a few feet, such as inside our cabinet, so we have to use some other protocol to bridge the distance between the host computer and the transputer system. The solution we adopted is the same as that used to connect the Photometrics PXL guider cameras; a pair of SCSI to fiber-optic converters extend the SCSI bus over the long distance. This extension is completely transparent to the host and transputer software.

The link from the host goes to the first transputer in the front end system, known as the root transputer, housed separately from the main crate. The function of the root transputer is to act as a router for messages from the host computer to the transputers, and for replies and data blocks going back to the host.

As well as acting as root transputer, this transputer monitors electronics cabinet temperatures, and controls and monitors the lamps in the calibration unit. It is housed in its own separate box, along

[1] DAQ15 and DAQ17, described in NEAN04 and NEAN05 respectively. DAQ15s acquire data from the A/D converters, and DAQ17s are used for clock generation, motor control and housekeeping.

with two TRAM[2] modules which give us RS232 capability. The RS232 transputers interface to the cryogenic temperature controller, an 8-channel cryogenic temperature readout, and a computer-controllable power strip. The power strip is used to control power to all the modules of the front end electronics system. Commands from one of the RS232 transputers can turn off power to everything else in the cabinet if there is a thermal problem, then turn everything back on when the problem is fixed. This is why the root and RS232 transputers are housed in their own enclosure with their own power supply.

From the root transputer box there are three branches of the transputer network. One has three motor controller transputers, and the other two control the spectrometer and slit-viewing cameras. The spectrometer camera section has one DAQ17 clock generator board and four DAQ15 acquisition boards. The slit-viewing camera (SCAM) uses one DAQ17 and one DAQ15.

3 Transputer network layout

A single transputer serial link consists of two signals, one in each direction. From cabinet to cabinet each is usually sent over twisted-pair cable, although over short distances such as along our backplane a single strand of wire wrap is OK (where “not OK” means “picks up noise and doesn't work”). As well as talking over up to four of these bi-directional links, each transputer interfaces to the others in the system via 3 “subsystem” signals, called **error**, **reset** and **analyze**, which daisychain from transputer to transputer.

A cable carries link 0 from the Matchbox, plus the subsystem signals, to the root transputer enclosure (aka the “housekeeping box”) where it connects to the root transputer's link 3. The root transputer connects to the three branches of the network on its links 0, 1 and 2. These three links and the subsystem signals come out of the housekeeping box on a DB37 connector. Another cable connects to another DB37 on the back of the main transputer crate. Inside the main transputer crate, the DB37 connector on the back links to the backplane, and wire wraps on the backplane interconnect the transputer boards in the crate.

The transputer network layout is shown in Figure 1. As we go from the host to the root transputer, then along each branch, note that the “upstream” link is link 0, and the “downstream” link is link 1. There is nothing special about any link; in fact they are completely identical except for the numbers. We merely chose this convention to keep things simple when writing the software. The transputer software protocol for the two camera sections mandates a couple of other simple conventions. First of all the clock generator transputer is nearest the host, since it passes on some messages, but not others, to the acquisition transputers (for instance a “go” message has meaning to the acquisition transputers but an “itime” does not). Secondly, the last acquisition transputer in each camera section has its “downstream” link looped back to link 2 of the clock transputer. This makes some of the message passing and handshaking simpler.

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[2] TRAM stands for TRansputer Application Module. A TRAM is a standard daughtercard used to package transputers with interfaces such as RS232 or SCSI.

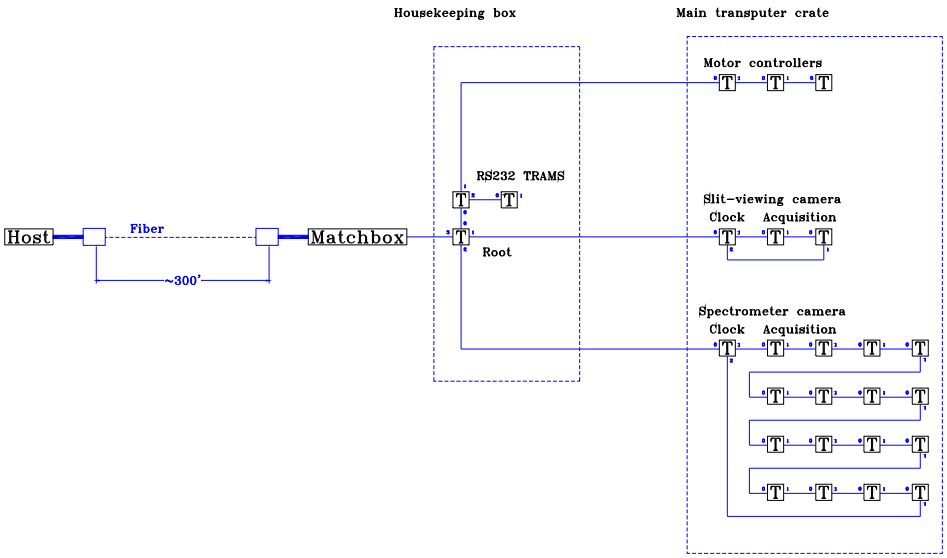

Figure 1: Transputer network layout

There are also logic signals (not shown in the picture) which are passed along from the clock generator to the acquisition transputers in each camera section. These signals are generated as part of the clock output which drives the detector arrays, and trigger the acquisition transputers to read data from the A-D converters on the analog boards.

4 Hardware details

4.1 Matchbox pinout

The MatchBox output connector pinout is shown in Figure 2. There are four links available from the MatchBox, but only one can be used by the software at any time. Our host software uses link 0.

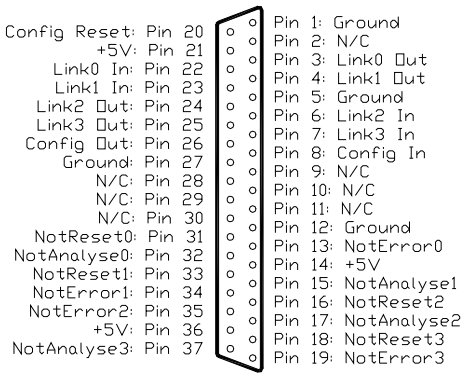

Figure 2: MatchBox links pinout

4.2 Housekeeping box

Inside the housekeeping box, the root transputer is on a DAQ17 board, which slides into card guides and has its front panel flush with the back of the box. The cable coming in from the MatchBox enters through a U-shaped hole, and is connected inside the box (this is for historical reasons to do with a failed method of making the long distance link). The two RS232 TRAMs are housed on a small board next to the DAQ17. They link to the root transputer as shown in Figure 1. Link 1 of the first serial transputer

and links 1 and 2 of the root transputer go to a DB25 connector on the back of the enclosure. They are on the same pins as links 0, 1, and 2 of the MatchBox in the pinout shown in Figure 2. The subsystem lines go to the same pins as the link 0 subsystem lines from the Matchbox. We then use a straight through cable to the main transputer enclosure. This makes the pinout from the housekeeping transputer look very similar to the MatchBox. This scheme helped us test the main transputer box, which was wired up before the housekeeping box was built.

4.3 Main transputer crate

4.3.1 DB37 to backplane

The DB37 connector is mounted on the crate's back panel, just behind the backplane, and connects to the backplane over twisted pair cables, with connectors which push onto the backplane pins.

4.3.2 Backplane links

Across the backplane everything is wire wrapped. Each transputer serial link comprises two wires, since the links are bidirectional. Subsystem signals (see below) are each on a single line daisy-chained along all the occupied slots. The data read signals are also on single wires. The details of the connections are shown in Figure 3 and listed in the tables at the end of this section.

The two types of transputer board (DAQ15 and DAQ17) have four transputers and one transputer respectively. There are no built-in links between the four on the DAQ15, so even the transputers on that style of board have to be connected to each other via the pins on the backplane.

In the motor controller section, which is a series of DAQ17s only, we just daisy-chain from link 1 of one board to link 0 of the next in line. There is no loopback at the end of the branch as in the camera sections. We have installed links for up to five motor controller boards, although we only have plans at the moment to install three in the crate.

In the slit-viewing camera section, we only use one of each type of board, and only two of the DAQ15's four transputers. We connect link 1 of the clock generator transputer (the DAQ 17) to link 0 of the first DAQ15 transputer (designated transputer A), link 1 of transputer A to link 0 of transputer B, and then from transputer B’s link 1 back to the clock generator transputer’s link 2.

In the spectrometer camera section, we do exactly the same, except that in this branch we have 4 DAQ15s, numbered 1 to 4, each with transputers A through D. We connect from link 1 of transputer 1D to link 0 on transputer 2A, and so on down the line. Again link 1 of the last acquisition transputer (4D) links back to link 2 of the clock generator.

Subsystem signals

In addition to the links there are three “subsystem” signals (reset, error and analyse) which must go to all the transputers. These are just three wires which daisy chain from board to board. The DAQ15 and DAQ17 boards have these signals on the same pins, and in the same order from top to bottom (reset, analyse, error), which makes the layout pretty simple.

Data read signal

In addition to all the transputer link and subsystem signals, there are also signals which need to pass from the clock generator (DAQ17) to the acquisition board(s) in each camera section. These signals are part of the clock waveform, and they tell the acquisition boards when to read data into their FIFO input buffers.

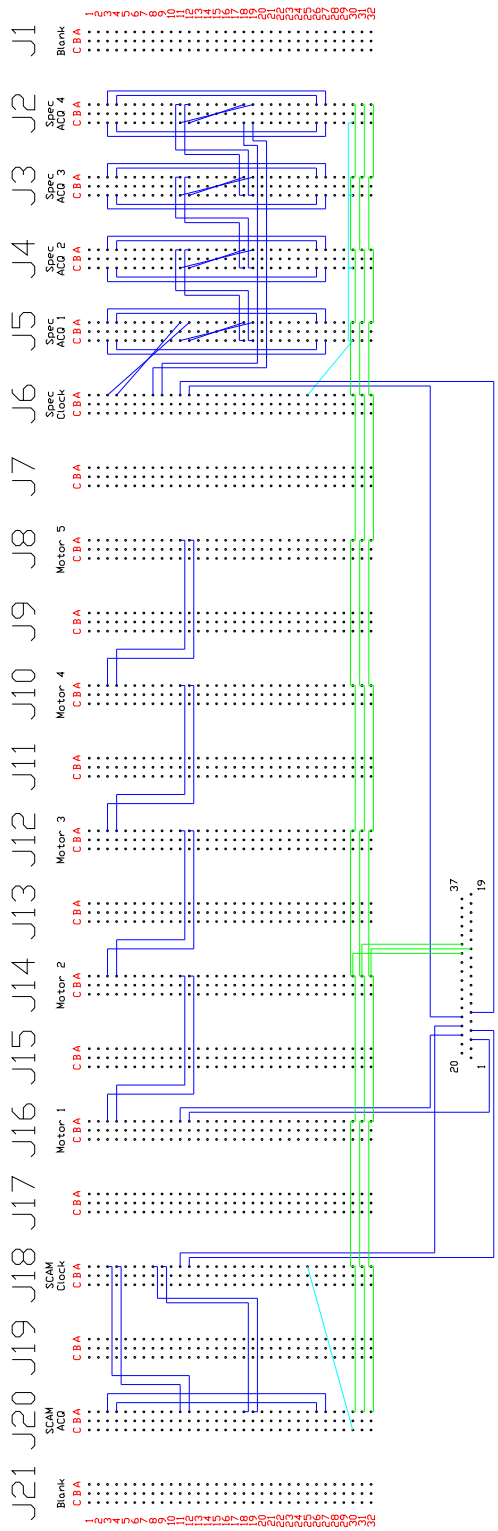

Figure 3: Backplane wiring

Connection lists

DB37 to backplane

	Connect	To	
Root out 0	DB37 - 3	J16 - A12	Motor 1 in 0
Root in 0	DB37 - 22	J16 - A11	Motor 1 out 0
Root out 1	DB37 - 4	J18 - A12	SCAM clock in 0
Root in 1	DB37 - 23	J18 - A11	SCAM clock out 0
Root out 2	DB37 - 24	J6 - A12	Spec. clock in 0
Root in 2	DB37 - 6	J6 - A11	Spec. clock out 0
NotReset0	DB37 - 31	J14 - A30	NotReset
NotAnalyse0	DB37 - 32	J14 - A31	NotAnalyse
NotError0	DB37 - 13	J14 - A32	NotError

Motor controller boards

	Connect	To	
Motor 1 out 1	J16 - A3	J14 - A12	Motor 2 in 0
Motor 1 in 1	J16 - A4	J14 - A11	Motor 2 out 0
Motor 2 out 1	J16 - A3	J14 - A12	Motor 3 in 0
Motor 2 in 1	J16 - A4	J14 - A11	Motor 3 out 0
Motor 3 out 1	J16 - A3	J14 - A12	Motor 4 in 0
Motor 3 in 1	J16 - A4	J14 - A11	Motor 4 out 0
Motor 4 out 1	J16 - A3	J14 - A12	Motor 5 in 0
Motor 4 in 1	J16 - A4	J14 - A11	Motor 5 out 0

Slit-viewing camera

	Connect	To	
Clock generator out 1	J18 - A3	J20 - A12	ACQ-A in 0
Clock generator in 1	J18 - A4	J20 - A11	ACQ-A out 0
ACQ-A out 1	J20 - A3	J20 - A27	ACQ-B in 0
ACQ-A in 1	J20 - A4	J20 - A26	ACQ-B out 0
ACQ-B out 1	J20 - A18	J18 - A9	Clock generator in 2
ACQ-B in 1B	J20 - A19	J18 - A8	Clock generator out 2

Spectrometer camera

	Connect	To	
Clock generator out 1	J6 - A3	J5 - A12	ACQ1-A in 0
Clock generator in 1	J6 - A4	J5 - A11	ACQ1-A out 0
ACQ1-A out 1	J5 - A3	J5 - A27	ACQ1-B in 0
ACQ1-A in 1	J5 - A4	J5 - A26	ACQ1-B out 0
ACQ1-B out 1	J5 - A18	J5 - C12	ACQ1-C in 0
ACQ1-B in 1	J5 - A19	J5 - C11	ACQ1-C out 0

ACQ1-C out 1	J5 - C3	J5 - C27	ACQ1-D in 0
ACQ1-C in 1	J5 - C4	J5 - C26	ACQ1-D out 0
ACQ1-D out 1	J5 - C18	J4 - A12	ACQ2-A in 0
ACQ1-D in 1	J5 - C19	J4 - A11	ACQ2-A out 0
ACQ2-A out 1	J4 - A3	J4 - A27	ACQ2-B in 0
ACQ2-A in 1	J4 - A4	J4 - A26	ACQ2-B out 0
ACQ2-B out 1	J4 - A18	J4 - C12	ACQ2-C in 0
ACQ2-B in 1	J4 - A19	J4 - C11	ACQ2-C out 0
ACQ2-C out 1	J4 - C3	J4 - C27	ACQ2-D in 0
ACQ2-C in 1	J4 - C4	J4 - C26	ACQ2-D out 0
ACQ2-D out 1	J4 - C18	J3 - A12	ACQ3-A in 0
ACQ2-D in 1	J4 - C19	J3 - A11	ACQ3-A out 0
ACQ3-A out 1	J3 - A3	J3 - A27	ACQ2-B in 0
ACQ3-A in 1	J3 - A4	J3 - A26	ACQ2-B out 0
ACQ3-B out 1	J3 - A18	J3 - C12	ACQ2-C in 0
ACQ3-B in 1	J3 - A19	J3 - C11	ACQ2-C out 0
ACQ3-C out 1	J3 - C3	J3 - C27	ACQ2-D in 0
ACQ3-C in 1	J3 - C4	J3 - C26	ACQ2-D out 0
ACQ3-D out 1	J3 - C18	J2 - A12	ACQ3-A in 0
ACQ3-D in 1	J3 - C19	J2 - A11	ACQ3-A out 0
ACQ4-A out 1	J2 - A3	J2 - A27	ACQ4-B in 0
ACQ4-A in 1	J2 - A4	J2 - A26	ACQ4-B out 0
ACQ4-B out 1	J2 - A18	J2 - C12	ACQ4-C in 0
ACQ4-B in 1	J2 - A19	J2 - C11	ACQ4-C out 0
ACQ4-C out 1	J2 - C3	J2 - C27	ACQ4-D in 0
ACQ4-C in 1	J2 - C4	J2 - C26	ACQ4-D out 0
ACQ4-D out 1	J2 - C18	J6 - A9	Clock generator in 2
ACQ4-D in 1	J2 - C19	J6 - A8	Clock generator out 2

Subsystem

	Connect	**To**
NotReset	J20 - A30	J18 - A30
	J18 - A30	J16 - A30
	J16 - A30	J14 - A30
	J14 - A30	J12 - A30
	J12 - A30	J10 - A30
	J10 - A30	J8 - A30
	J8 - A30	J6 - A30
	J6 - A30	J5 - A30
	J5 - A30	J4 - A30
	J4 - A30	J3 - A30
	J3 - A30	J2 - A30
NotAnalyse	J20 - A31	J18 - A31

	J18 - A31	J16 - A31
	J16 - A31	J14 - A31
	J14 - A31	J12 - A31
	J12 - A31	J10 - A31
	J10 - A31	J8 - A31
	J8 - A31	J6 - A31
	J6 - A31	J5 - A31
	J5 - A31	J4 - A31
	J4 - A31	J3 - A31
	J3 - A31	J2 - A31
NotError	J20 - A32	J18 - A32
	J18 - A32	J16 - A32
	J16 - A32	J14 - A32
	J14 - A32	J12 - A32
	J12 - A32	J10 - A32
	J10 - A32	J8 - A32
	J8 - A32	J6 - A32
	J6 - A32	J5 - A32
	J5 - A32	J4 - A32
	J4 - A32	J3 - A32
	J3 - A32	J2 - A32

Data read signals

	Connect	**To**	
SCAM			
Clock generator FIFORd out	J18 - A25	J20 - C30	ACQ FIFORd in
Spectrometer			
Clock generator FIFORd out	J6 - A25	J5 - C30	ACQ1 FIFORd in
ACQ1 FIFORd in	J5 - C30	J4 - C30	ACQ2 FIFORd in
ACQ2 FIFORd in	J4 - C30	J3 - C30	ACQ3 FIFORd in
ACQ3 FIFORd in	J3 - C30	J2 - C30	ACQ4 FIFORd in