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NIRSPEC Electronics Application Note 10.00
Level Shifter Box Description and Test Specification

1. Introduction

This document describes the performance of the level shifter box, and provides a functional test procedure. The level shifter box is the intermediary between the DAQ17 Clock Generator Boards and the Detector Head Clock Inputs. For more information about these components, see NEDN 17.00 (DAQ17 board) and NEDN 04.00 and 10.00 (Detector Clocks). The level shifter board has three functions. First, it sends clock pulse signals to the detector, by using DAQ17 TTL pulses as a trigger for solid state switches. These switches toggle between voltages generated on the board to create output clock signals. Second, the ALADDIN level shifter box also buffers Tend signals from the ALADDIN detector for diagnostic testing. Third, the board also sends the individual power

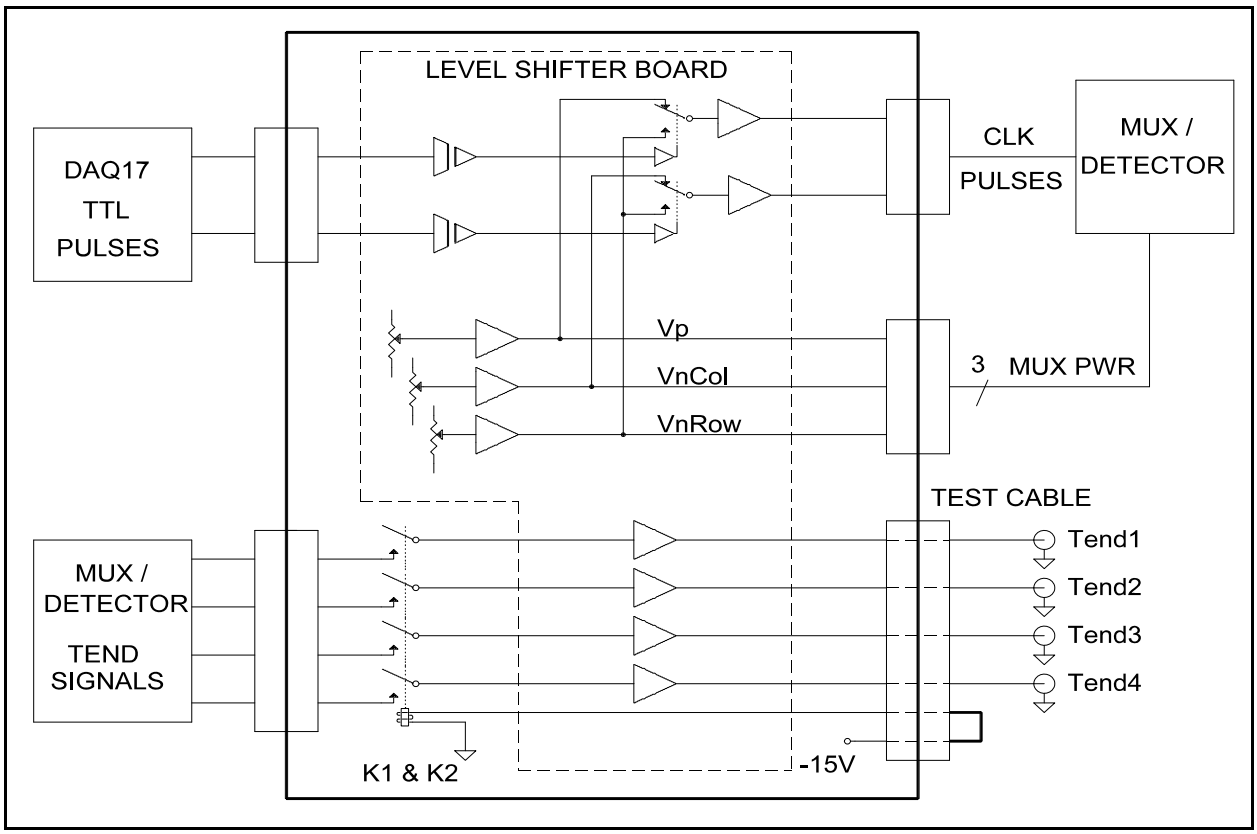

Figure 1. Level Shifter Box and Board Block Diagram

voltages to the detector multiplexers. The PICNIC and ALADDIN detectors have separate Level Shifter boards which have differences in physical layout, because the detectors have different clock pulse requirements.

2. General Description

2.1 Grounds

The level shifter board has three types of ground: analog ground (AGND), digital ground (DGND), and computer ground (CGND). Analog and digital ground are separated until they connect at the bottom of the pc board near the P2 connector, in order to keep the digital transient noise from affecting the analog ground on the board. Computer ground is electrically and physically separated from the rest of the board by the ISO150 capacitive isolators. By protecting the analog and digital ground from computer ground interference, we eliminate ground loops and cross talk to the analog circuit.

2.2 DC Output Clock Voltages

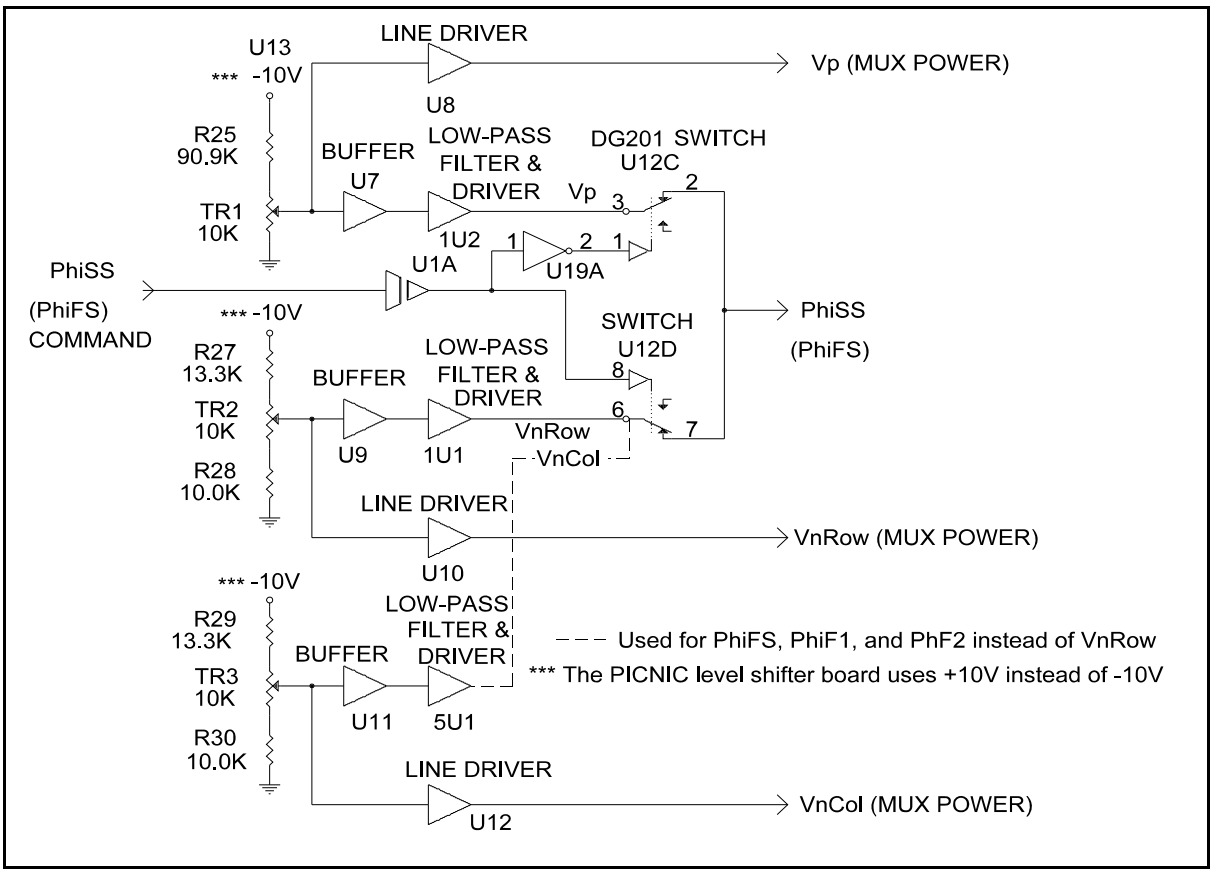

Figure 2. DC Output Clock Voltage Circuit Diagram

Each voltage is generated through a voltage divider supplied by the AD587 10VDC voltage

source U13, as shown in Figure 2. In the ALADDIN board, the +10V supply is inverted by OP27 U14 to have -10V for the dividers. These voltage levels can be varied by adjusting a 10KΩ trimpot (TR1, TR2, TR3). They are then buffered with an OP27 (U7, U9, U11), low pass filtered with an RC circuit (i.e., 1R1 & 1C1), line driven with an HA5002 driver with current limiting resistors (i.e., 1U1, 1R3, 1R5), then sent to the DG201HS solid state switches (U21 to U26). The diodes (i.e., 1D1 for the clock signals) prevent the detector from receiving clock voltages that are the wrong polarity. The capacitors C94 and C95 (not shown on Figure 2, see schematic) help prevent cross talk by compensating for voltage drops which occur when switches U23 and U24 are activated, because their voltage inputs are tied together. The ALADDIN detector needs three clock voltages (VnRow, VnCol, and Vp), while the PICNIC detector needs two (Vdd and Vss). The voltage levels for each detector's clock signals can be found on Table 2. Since fewer clock voltages are required for the PICNIC detector, its level shifter board does not use potentiometer TR3, line drivers 5U1 through 8U2, or switches U25 and U26.

The level shifter board also sends these clock voltages to the detector multiplexers. As shown in Figure 2, the voltage is sent to an HA5002 driver (U8, U10, U12) and then through P2 to the detectors. The diodes (D1 through D5) prevent a voltage with wrong polarity from going to the detector. In the ALADDIN and PICNIC board, the diodes have opposite orientations, since the ALADDIN detector needs negative clock voltages, and the PICNIC detector requires positive voltages.

Table 1. Pin Assignments for Detector Clocks

Pin Number	ALADDIN Level Shifter	PICNIC Level Shifter	Pin Number	ALADDIN Level Shifter	PICNIC Level Shifter
P1-C1	Phi-SS	Pixel	P1-C16	Phi-F2	N/A
P1-C3	Phi-S1	Read	P1-C21	Phi-DES1	LSync
P1-C6	Phi-S2	Line	P1-C23	Phi-DES2	FSync
P1-C8	Phi-E/O	Reset	P1-C26	Phi-DES3	N/A
P1-C11	Phi-FS	N/A	P1-C28	Phi-DES4	N/A
P1-C13	Phi-F1	N/A			

2.3 Clock Signal Circuits

The Clock circuits convert DAQ17 TTL pulses into the clocking levels for the detectors. As shown in Figure 2, each of these pulses travels through ISO150 capacitive isolators (U1 through U6) to trigger a pair of DG201HS solid state switches (U21 through U26). The TTL pulse goes straight to the trigger of one switch, and the other switch has the signal inverted by a 74HC04A inverter (U19, U20, U29). These normally-open switches are activated by a low voltage at the trigger. When the DAQ17 signal is TTL "high," the switch that has the inverter is activated and allows its associated voltage to travel to the detector. The switch without the inverter turns on when the TTL clock pulse goes "low." This switching circuitry produces the output detector clock voltage pulses. A listing of the Clocks for each detector can be found in Table 1. As shown in Table 2, a low input

DAQ17 TTL signal in the ALADDIN Clock circuit activates the Vp switch, sending -0.2V to the detector, and a high signal activates the VnRow or VnCol switch, which sends either -5.6V or -6.0V to the detector (see Table 2). When the PICNIC Clock circuits for Pixel, Read, Line, or Reset signals receive a low TTL pulse, Vss = 0.0V is sent to the output, while a high TTL input routes Vdd = +5.0V to the output. For the LSync or FSync signal of the PICNIC circuit, Vdd is sent to the output when a "high" pulse is received, and Vss is sent when the switch gets a "low" pulse. The PICNIC detector has fewer clock signals, and its level shifter board does not utilize line drivers 5U1 through 8U2, or switches U24 through U26.

Table 2. Level Shifter Output Clock Values

DAQ17 TTL Clock Pulse	ALADDIN Detector Clocks		PICNIC Detector Clocks	
	Phi-SS Phi-DES1 Phi-E/O Phi-S1 Phi-DES2 Phi-DES4 Phi-S2 Phi-DES3	Phi-FS Phi-F1 Phi-F2	Pixel Read Line Reset	LSync FSync
Low	Vp = -0.2V	Vp = -0.2V	Vss = 0.0V	Vdd =5.0V
High	VnRow = -5.6V	VnCol=-6.0V	Vdd = 5.0V	Vss = 0.0V

2.6 Tend Circuit (ALADDIN Board only)

The Tend signals are diagnostic output signals from each ALADDIN detector quadrant. The four signals enter the level shifter box and go to relays K1 and K2. These relays are activated when the Tend connector plug (E0-P3) is attached to the box. As shown in figure 3, the E0-P3 connector has a loop which connects -15V to the relay. Without the connector, the relay does not receive the supply voltage, keeping the circuit open. This arrangement sends the Tend signals to the level shifter board only when the connector is present. In this way, the loading on the detector from the diagnostic signals can be kept to a minimum. The Tend signals require a 10kΩ pull up resistor load to -3V, which is made from a resistor network of two 20kΩ resistors (R35 through R42) and VnCol / 2 (= -6.0V / 2 through a voltage divider circuit). The signals are then buffered through HA5002 line drivers (U15 through U18) and sent off of the board through P2 to the box connector E0-J3, which goes to four external BNC test points.

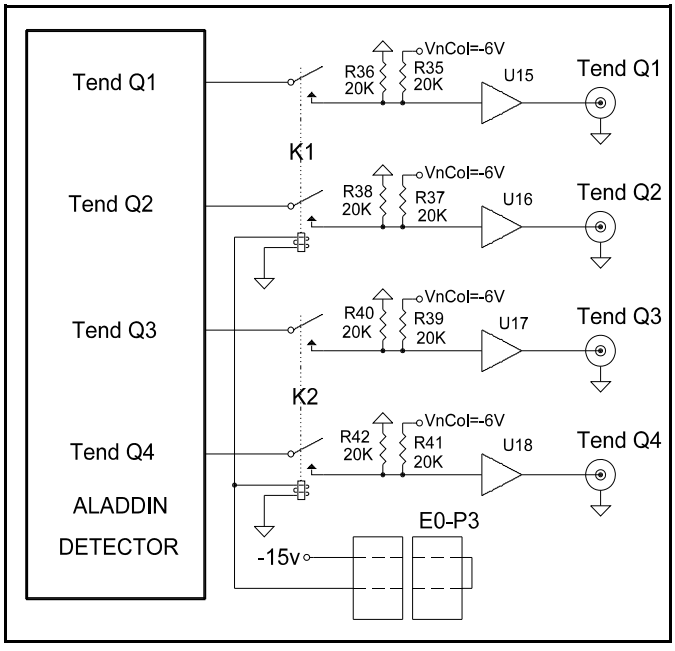

Figure 3. Tend Circuit Diagram

2.7 1024 Level Shifter Board Configuration

2.7.1 Components not installed

R1 - R24
D4, D5
J1, J4, J6

2.7.2 Board Modifications

U26 pin 11 track cut right after pin
8U2 pin 8 track cut right after pin
U26 pin 6 track cut right after pin
7U1 pin 8 track cut right before it passes adjacent to TP33
U25 pin 11 track cut right after pin
6U2 pin 8 track cut right after pin
U25 pin 6 track cut right after pin
5U1 pin 8 track cut right before it passes adjacent to TP29
U22 pin 11 track cut right after pin
4U2 pin 8 track cut right after pin
U22 pin 6 track cut right after pin
3U1 pin 8 track cut right before it passes adjacent to TP25
U21 pin 11 track cut right after pin
2U2 pin 8 track cut right after pin
U21 pin 6 track cut right after pin
1U1 pin 8 track cut right before it passes adjacent to TP21
Jumper wire from U26 pin 6 to track connected to 7U1 pin 8
Jumper wire from U26 pin 11 to 8U2 pin 8
Jumper wire from U25 pin 6 to track connected to 5U1 pin 8
Jumper wire from U25 pin 11 to 6U2 pin 8
Jumper wire from U22 pin 6 to track connected to 3U1 pin 8
Jumper wire from U22 pin 11 to 4U2 pin 8
Jumper wire from U21 pin 6 to track connected to 1U1 pin 8
Jumper wire from U21 pin 11 to 2U2 pin 8
TP34 connected to TP35 track
TP33 connected to TP32 track
TP30 connected to TP31 track
TP29 connected to TP28 track
TP26 connected to TP27 track
TP23 connected to TP22 track
TP22 connected to TP23 track
TP21 connected to TP20 track

2.7.3 Jumpers Installed

J2, J3

J5 and J6 only used with the Spare circuit

2.8 256 Level Shifter Board Configuration

2.8.1 Components not installed

R1 - R24, R29, R30, R34
TR3
C16
D3, D4, D5
U4, U6, U12, U14 - U18, U24 - U26, 5U1- 8U1, 5U2 - 8U2, 24U1, 25U1, 26U1, 28U1 30U1
J2, J3

2.8.2 Board Modifications

Jumper wire between U9 pin 3 & U11 pin 3
1MΩ installed across D7, D11, D1, D2
D8, D9, D10, D12 shorted
R61, R62 changed to 301K

2.8.3 Jumpers Installed

J1, J4

2.8.4 Other Modifications

All diodes installed with polarity opposite to the silkscreen

3. Functional Test Specification and Test Acceptance Procedure for PICNIC Level Shifter Board S/N:_____

3.1 Test Equipment Needed

Oscilloscope
Digital Multimeter
Function Generator
DC Power Supply

3.2 Drawing List

PICNIC Level Shifter Board Schematic: 603017
Level Shifter Board Assembly Drawing: 603008

3.3 Power Supply Connection

Provide the following DC voltages and grounds to the proper pins on the board. Measure the power supply current.
* Power Supply for isolated computer section of board ** Static Current

Power Supply	Board Connection	Ground Connection	**Nominal Current	Measured Current
+5 ± 0.05 VDC	P2-C13	P2-A31	80 mA	mA
+15 ± 0.2 VDC	P2-C21	P2-A31	170 mA	mA
-15 ± 0.2 VDC	P2-C17	P2-A31	150 mA	mA
+5* ± 0.1 VDC	P1-C30	P1-A32	5 mA	mA

3.4 Voltage Source Verification

Measure	Description	Specification	Result
TP19 (J1 & J4 installed)	AD587 (U13) Output	+10.00±0.05VDC	VDC

3.5 DC Output Clock Voltages

This test will check the voltage divider (TR1, TR2) and verify the correct voltage range for the output clocks.

*Counter-Clockwise **Clockwise

Description	Measure	Specification	Results
Adjust TR1 fully CCW*	TP13, TP14	0.0 ± 0.2 VDC	VDC
Adjust TR1 fully CW**	TP13, TP14	+6.0 ± 0.1VDC	VDC
Adjust TR2 fully CCW	TP15, TP16	0.0 ± 0.2 VDC	VDC
Adjust TR2 fully CW	TP15, TP16	+6.0 ± 0.2VDC	VDC

3.6 Isolator Test

This test will verify that the ISO150 isolators (U1, U2, U5) are functioning properly. Apply a TTL (0 to 5V square wave) 1.0 ± 0.1 MHz to each of the following TTL Inputs, and verify that the output is of the same phase and voltage level as the input.

1MHz TTL Input	Measure	Verify Output
P1-C1 (Pixel)	TP1	TTL 0° _____
P1-C3 (Read)	TP2	TTL 0° _____
P1-C6 (Line)	TP3	TTL 0° _____
P1-C8 (Reset)	TP4	TTL 0° _____
P1-C21 (LSync)	TP9	TTL 0° _____
P1-C23 (FSync)	TP10	TTL 0° _____

3.7 Buffer Test

This test verifies the correct operation of the HA5002 buffer circuits (U27, U28, 1U1 through 4U2). Adjust TR1 until TP13 = +5.0 ± 0.1 VDC; adjust TR2 until TP15 = 0.0 ± 0.1 VDC

Measure	Specification	Results
TP20	0.0 ± 0.1 VDC	VDC
TP21	+5.0 ± 0.1 VDC	VDC
TP22	0.0 ± 0.1 VDC	VDC
TP23	+5.0 ± 0.1 VDC	VDC
TP24	0.0 ± 0.1 VDC	VDC
TP25	+5.0 ± 0.1 VDC	VDC
TP26	0.0 ± 0.1 VDC	VDC
TP27	+5.0 ± 0.1 VDC	VDC
TP36	0.0 ± 0.1 VDC	VDC
TP37	+5.0 ± 0.1 VDC	VDC

3.8 PICNIC Clock Circuit Test

This test will verify that the ISO150 capacitive isolators (U1, U2, U3, U5), the HA5002 buffers (1U1 through 4U2, U27, U28), the 74HC04A digital inverters (U19, U20) and the DG201HS solid state switches (U21 through U23) are functioning properly by verifying the voltage levels and the phase with respect to the TTL input.

Apply +5v* to Isolator Section, with P3-C30 (+5V*) and P3-A32 (CGND).

Adjust TR1 until TP13 = +5.0 ± 0.1 VDC; adjust TR2 until TP15 = 0.0 ± 0.1 VDC

Apply a TTL pulse (0 to 5V square wave) at f =1.0 ± 0.1 MHz to each of the following TTL Inputs:

1MHz TTL Input	Measure	Specification	Phase	Results
P1-C1 (Pixel)	P2-C1	Level 1 = +5.0 ± 0.1 VDC Level 2 = 0.0 ± 0.1 VDC	0°	Level1 _____VDC Level2 _____VDC
P1-C3 (Read)	P2-C2	Level 1 = +5.0 ± 0.1 VDC Level 2 = 0.0 ± 0.1 VDC	0°	Level1 _____VDC Level2 _____VDC
P1-C6 (Line)	P2-C3	Level 1 = +5.0 ± 0.1 VDC Level 2 = 0.0 ± 0.1 VDC	0°	Level1 _____VDC Level2 _____VDC
P1-C8 (Reset)	P2-C4	Level 1 = +5.0 ± 0.1 VDC Level 2 = 0.0 ± 0.1 VDC	0°	Level1 _____VDC Level2 _____VDC
P1-C21 (LSync)	P2-C5	Level 1 = +5.0 ± 0.1 VDC Level 2 = 0.0 ± 0.1 VDC	180°	Level1 _____VDC Level2 _____VDC
P1-C23 (FSync)	P2-C6	Level 1 = +5.0 ± 0.1 VDC Level 2 = 0.0 ± 0.1 VDC	180°	Level1 _____VDC Level2 _____VDC

4. Functional Test Specification and Test Acceptance Procedure for ALADDIN Level Shifter Board S/N:_____

4.1 Test Equipment Needed

Oscilloscope
Digital Multimeter
Function Generator
DC Power Supply

4.2 Drawing List

ALADDIN Level Shifter Board Schematic: 603007
ALADDIN Level Shifter Board Assembly Drawing: 603008

4.3 Power Supply Connection

Provide the following DC voltages and grounds to the proper pins on the board. Measure the power supply current.
* Power Supply for isolated computer section of board ** Static Current

Power Supply	Board Connection	Ground Connection	**Nominal Current	Measured Current
+5 ± 0.05 VDC	P2-C13	P2-A31	50 mA	mA
+15 ± 0.2 VDC	P2-C21	P2-A31	250 mA	mA
-15 ± 0.2 VDC	P2-C17	P2-A31	200 mA	mA
+5* ± 0.1 VDC	P1-C30	P1-A32	5 mA	mA

4.4 Voltage Source Verification

Measure	Description	Specification	Result
TP19 (J2 & J3 installed)	Inverted AD587 (U13) Output	-10.00±0.05VDC	VDC

4.5 DC Output Clock Voltages

This test will check the voltage divider (TR1, TR2, TR3), the OP27 filters (U7, U9, U11), the HA5002 buffers (U8, U10, U12) and verify the correct voltage range for the output clocks.

*Counter-Clockwise **Clockwise

Description	Measure	Specification	Results
Adjust TR1 fully CCW*	TP13, TP14	0.0 ± 0.2 VDC	VDC
Adjust TR1 fully CW**	TP13, TP14	- 1.0 ± 0.2 VDC	VDC
Adjust TR2 fully CCW	TP15, TP16	-3.0 ± 0.3 VDC	VDC
Adjust TR2 fully CW	TP15, TP16	-6.0 ± 0.3 VDC	VDC
Adjust TR3 fully CCW	TP17, TP18	-3.0 ± 0.3 VDC	VDC
Adjust TR3 fully CW	TP17, TP18	-6.0 ± 0.3 VDC	VDC

4.6 Isolator Test

This test will verify that the ISO150 isolators (U1 through U6) are functioning properly. Apply a TTL (0 to 5V square wave) 1.0 ± 0.1 MHz to each of the following TTL Inputs, and verify that the output is of the same phase and voltage level as the input.

1MHz TTL Input	Measure	Verify Output
P1-C1 (Phi-SS)	TP1	TTL 0° _____
P1-C3 (Phi-S1)	TP2	TTL 0° _____
P1-C6 (Phi-S2)	TP3	TTL 0° _____
P1-C8 (Phi-E/O)	TP4	TTL 0° _____
P1-C11 (Phi-FS)	TP5	TTL 0° _____
P1-C13 (Phi-F1)	TP6	TTL 0° _____
P1-C16 (Phi-F2)	TP7	TTL 0° _____
P1-C18 (Spare)	TP8	TTL 0° _____
P1-C21 (Phi-DES1)	TP9	TTL 0° _____
P1-C23 (Phi-DES2)	TP10	TTL 0° _____
P1-C26 (Phi-DES3)	TP11	TTL 0° _____
P1-C28 (Phi-DES4)	TP12	TTL 0° _____

4.7 Clock Circuit Test

This test will verify that the HA5002 buffers (U27, U28, 1U1& 1U2 through 7U1, 7U2), the 74HC04A digital inverters (U19, U20, U29) and the DG201HS solid state switches (U21 through U26) are functioning properly by verifying the output clock voltage levels and phase with respect to the input TTL signal. Apply +5v* to Isolator Section, with P3-C30 (+5V*) and P3-A32 (CGND). Adjust TR1 until TP13 = -0.2 ± 0.1 VDC; adjust TR2 until TP15 = -5.6 ± 0.1 VDC; adjust TR3 until TP17 = -6.0 ± 0.1 VDC. Apply a TTL (0 to 5V square wave) 1.0 ± 0.1 MHz to each of the following TTL Inputs:

1MHz TTL Input	Measure	Specification	Phase	Results
P1-C1 (Phi-SS)	P2-C1	Level 1 = -0.2 ± 0.2 VDC Level 2 = -5.6 ± 0.2 VDC	180°	Level1 _____VDC Level2 _____VDC
P1-C3 (Phi-S1)	P2-C2	Level 1 = -0.2 ± 0.2 VDC Level 2 = -5.6 ± 0.2 VDC	180°	Level1 _____VDC Level2 _____VDC
P1-C6 (Phi-S2)	P2-C3	Level 1 = -0.2 ± 0.2 VDC Level 2 = -5.6 ± 0.2 VDC	180°	Level1 _____VDC Level2 _____VDC
P1-C8 (Phi-E/O)	P2-C4	Level 1 = -0.2 ± 0.2 VDC Level 2 = -5.6 ± 0.2 VDC	180°	Level1 _____VDC Level2 _____VDC
P1-C11 (Phi-FS)	P2-C9	Level 1 = -0.2 ± 0.2 VDC Level 2 = -6.0 ± 0.2 VDC	180°	Level1 _____VDC Level2 _____VDC
P1-C13 (Phi-F1)	P2-C10	Level 1 = -0.2 ± 0.2 VDC Level 2 = -6.0 ± 0.2 VDC	180°	Level1 _____VDC Level2 _____VDC
P1-C16 (Phi-F2)	P2-C11	Level 1 = -0.2 ± 0.2 VDC Level 2 = -6.0 ± 0.2 VDC	180°	Level1 _____VDC Level2 _____VDC
P1-C21 (Phi-DES1)	P2-C5	Level 1 = -0.2 ± 0.2 VDC Level 2 = -5.6 ± 0.2 VDC	180°	Level1 _____VDC Level2 _____VDC

4.8 Clock Circuit Test (Cont.)				
1MHz TTL Input	Measure	Specification	Phase	Results
P1-C23 (Phi-DES2)	P2-C6	Level 1 = -0.2 ± 0.2 VDC Level 2 = -5.6 ± 0.2 VDC	180°	Level1 _____VDC Level2 _____VDC
P1-C26 (Phi-DES3)	P2-C7	Level 1 = -0.2 ± 0.2 VDC Level 2 = -5.6 ± 0.2 VDC	180°	Level1 _____VDC Level2 _____VDC
P1-C28 (Phi-DES4)	P2-C8	Level 1 = -0.2 ± 0.2 VDC Level 2 = -5.6 ± 0.2 VDC	180°	Level1 _____VDC Level2 _____VDC
P1-C18 (Spare) J5 installed, J6 open	P2-C12	Level 1= -0.2 ± 0.2 VDC Level 2 = -5.5 ± 0.2 VDC	0°	Level1 _____VDC Level2 _____VDC
P1-C18 (Spare) J6 installed, J5 open	P2-C12	Level 1 = -0.2 ± 0.2 VDC Level 2 = -6.0 ± 0.2 VDC	0°	Level1 _____VDC Level2 _____VDC

4.9 Tend Circuit

This test will verify that the tend circuit is connected correctly and the HA5002 buffers (U15 through U18) are functioning properly. Send a 4.0 ± 0.02 vP-P sinewave centered at 0V at f = 1.0 ± 0.1 MHz to the following inputs:

4vP-P 1MHz Sinewave Input	Measure	Specification	Result
P2-C27 (Q1-TEND)	BNC1, P2-C31	4.0 ± 0.02 vP-P at 0V	vP-P
P2-C28 (Q2-TEND)	BNC2, P2-C32	4.0 ± 0.02 vP-P at 0V	vP-P
P2-C29 (Q3-TEND)	BNC3, P2-B32	4.0 ± 0.02 vP-P at 0V	vP-P
P2-C30 (Q4-TEND)	BNC4, P2-A32	4.0 ± 0.02 vP-P at 0V	vP-P