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NIRSPEC Electronics Application Note 09.00
PICNIC Bias Board Description and Test Specification

1. Introduction

This document describes the performance of the PICNIC bias board, and provides a functional test procedure. The bias board is the intermediary between the DAQ17 Clock Generator Board and the Detector Head Bias Input. Additional information on these two components can be found in documents NEDN 22.00 (PICNIC Detector) and NEDN 17.00 (DAQ17 Board). The board produces fixed bias voltages that are sent to the detectors.

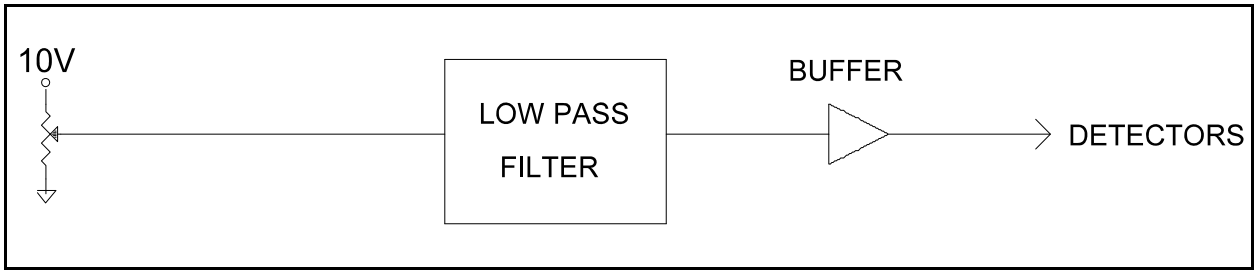

Figure 1. PICNIC Bias Board Block Diagram

2. General Board Description

2.1 Grounds

The bias board has three types of ground: analog ground (AGND), digital ground (DGND), and computer ground (CGND). Analog and digital ground are separated until they connect at the bottom of the pc board near the P2 connector, in order to keep the digital transient noise from affecting the analog ground on the board. Computer ground is electrically and physically separated from the rest of the board by the ISO150 capacitive isolators. By protecting the analog and digital ground from computer ground interference, we eliminate ground loops and cross talk to the analog circuit.

2.2 Bus Connections

The Bias boards use Sun style VME bus connections (labeled P1 and P2 on the board, P2 and P3 on the backplane). Because of this bus structure, these signals are automatically connected to all the preamp boards connected to the backplane bus. The power connections come to the board from the backplane bus through P2.

2.3 Fixed Bias Voltages

The Fixed bias circuit provides the stable bias voltages needed for both detectors. The nine Fixed bias voltages for the PICNIC detector (High, Low, CellDrain, MuxSub, Vreset, Drain, BiasPwr, BiasGate, and DSub) come from voltage divider circuits supplied by an AD587 +10VDC supply (U10), as shown in Figure 2. The bias voltage levels are adjusted with a potentiometer accessible from the front panel (TR1 through TR7, TR9, TR11), low pass filtered (17U1 through 20U1, 23U1 through 28U1) and then sent to the backplane bus to the bias input on the detectors. The diodes (D1 through D12) prevent the detectors from receiving the wrong voltage polarity. The value range of each bias voltage is found in Table 1. For more information about the PICNIC Bias voltages, see NEDN 22.00.

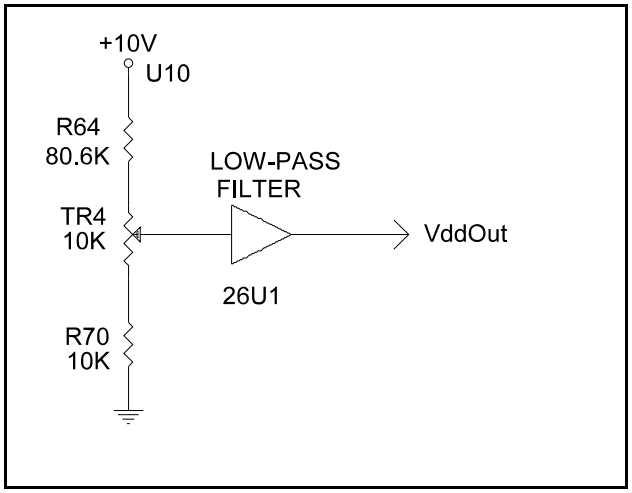

Figure 2. Fixed Bias Voltage Circuit

Table 1. PICNIC Fixed Bias Voltages

PICNIC Fixed Bias Signals	Board Voltage Range	Nominal Values
High	4.0 - 6.0 V	+5.0 V
Low	0.0 - 1.0 V	0.0 V
CellDrain	0.0 - 1.0 V	0.0 V
MuxSub	0.0 - 1.0 V	0.0 V
Vreset	0.0 - 2.0 V	0.5 - 1.0 V
Drain	0.0 - 1.0 V	0.0 V
BiasPwr	4.0 - 6.0 V	5.0 V
BiasGate	2.7 - 4.3 V	3.2 - 3.8 V
DSub	0.0 - 1.0 V	0.0 V

2.4 PICNIC Bias Board Configuration

2.4.1 Components not installed

U1 - U15, U17 - U19, 0U1 - 4U1, 6U1, 8U1, 10U1, 12U1 -16U1, 29U1

TR8, TR10, TR12, TR 14- TR16
R1-R20, R22, R24, R26, R28 - R30, R32 - R34, R36, R38 - R40
C24, C97-C99
J2, J3, J5 through J12, JRdy

2.4.2 Board Modifications

Jumper wire soldered on U12 between pins 2 & 3
Jumper wire soldered on U12 between pins 14 & 15
Jumper wire soldered on U13 between pins 2 & 3
Jumper wire soldered on U13 between pins 14 & 15
Jumper wire soldered on U7 between pins 6 & 7
Jumper wire soldered on U7 between pins 13 & 14
Track cut at U7 pin 10
1MΩ installed across D4
D2 shorted and removed

2.4.3 Jumpers Installed

J1, J4

2.4.4 Other Modifications

D1 - D15 polarity is opposite from the silkscreen indication

3. Functional Test Specification and Test Acceptance Procedure for PICNIC Bias Board S/N:_____

3.2 Test Equipment Needed
Oscilloscope
Digital Multimeter
Function Generator
DC Power Supply

3.1 Drawing List
PICNIC Bias Board Schematic: 603015
Bias Board Assembly Diagram: 603006

3.3 Power Supply Connection
Provide the following DC voltages and grounds to the proper pins on the board. Record the current from the power supply display.
* Power Supply for isolated computer section of board ** Static Current

Power Supply	Board Connection	Ground Connection	**Nominal Current	Measure Current
+15 ± 0.2 VDC	P2-C26	P2-C1	35 mA	mA
-15 ± 0.2 VDC	P2-C28	P2-C1	40 mA	mA

3.4 Voltage Source Verification

Measure	Description	Specification	Result
TP12 (J1 and J4 installed)	AD587 (U10) Output	+10.00±0.05VDC	VDC

3.5 Fixed Bias Circuit

This test will verify the voltage range and set the correct voltage levels of the fixed bias circuits (TR1 through TR7, TR9, TR17).
*CCW = Counter-Clockwise **CW = Clockwise

Test Conditions	Measure	Specification	Results
Adjust TR1 fully CCW*	TP39 P1-C1	+4.0 ± 0.2 V	VDC
Adjust TR1 fully CW**		+6.0 ± 0.2 V	VDC
Adjust TR1 so TP39 =+5.0 ± 0.1V (High)		+5.0 ± 0.1V	VDC
Adjust TR2 fully CCW.	TP40 P1-C6	0.0 ± 0.1 V	VDC
Adjust TR2 fully CW.		-10.0 ± 0.1 V	VDC
Adjust TR2 so TP40 = 0.0 ± 0.1V (Low)		0.0 ± 0.1V	VDC
Adjust TR3 fully CCW	TP41 P1-C12	0.0 ± 0.1 V	VDC
Adjust TR3 fully CW		+1.0 ± 0.1 V	VDC
Adjust TR3 so TP41= 0.0 ± 0.1V (Cell Drain)		0.0 ± 0.1V	VDC
Adjust TR4 fully CCW	TP42 P1-C18	0.0 ± 0.1 V	VDC
Adjust TR4 fully CW		+1.0 ± 0.1 V	VDC
Adjust TR4 so TP42= 0.0±0.1V (MuxSub)		0.0±0.1V	VDC
Adjust TR5 fully CCW.	TP43 P1-C25	0.0 ± 0.1 V	VDC
Adjust TR5 fully CW.		+2.0 ± 0.1 V	VDC
Adjust TR5 so TP43 = +0.75 ± 0.1V (Vreset)		+0.75 ± 0.1V	VDC

3.5 Fixed Bias Circuit (Cont.)			
Test Conditions	Measure	Specification	Results
Adjust TR6 fully CCW.	TP44 P1-C31	0.0 ± 0.1 V	VDC
Adjust TR6 fully CW.		+1.0 ± 0.1 V	VDC
Adjust TR6 so TP44 =0.0 ± 0.1 V (Drain)		0.0 ± 0.1 V	VDC
Adjust TR17 fully CCW	TP35 P2-B21	0.0 ± 0.1 V	VDC
Adjust TR17 fully CW		+1.0 ± 0.1 V	VDC
Adjust TR17 so TP35= 0.0 ± 0.1V (Dsub)		0.0 ± 0.1V	VDC
Adjust TR7 fully CCW	TP45 P2-B5	+4.0 ± 0.1 V	VDC
Adjust TR7 fully CW		+6.0 ± 0.1 V	VDC
Adjust TR7 so TP15=+5.0 ± 0.1V (BiasPwr)		+5.0 ± 0.1V	VDC
Adjust TR9 fully CCW	TP46 P2-B7	+2.7 ± 0.1 V	VDC
Adjust TR9 fully CW		+4.3 ± 0.1 V	VDC
Adjust TR9 so TP17=+3.5± 0.1V (BiasGate)		+3.5± 0.1V	VDC