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NIRSPEC Electronics Application Note 08.00
ALADDIN Bias Board Description and Test Specification

1. Introduction

This document describes the performance of the ALADDIN bias board, and provides a functional test procedure. The bias board is the intermediary between the DAQ17 Clock Generator Board and the Detector Head Bias Input. Additional information on these two components can be found in documents NEDN 10.00 (ALADDIN Detector) and NEDN 17.00 (DAQ17 Board). The board has two functions. First, fixed bias voltages are generated on the board are sent to the detectors. Second, switchable bias voltages are converted from DAQ17 TTL pulses and sent to the detectors. The switchable bias circuit also has a latch to control the VdetCom voltage level.

2. General Board Description

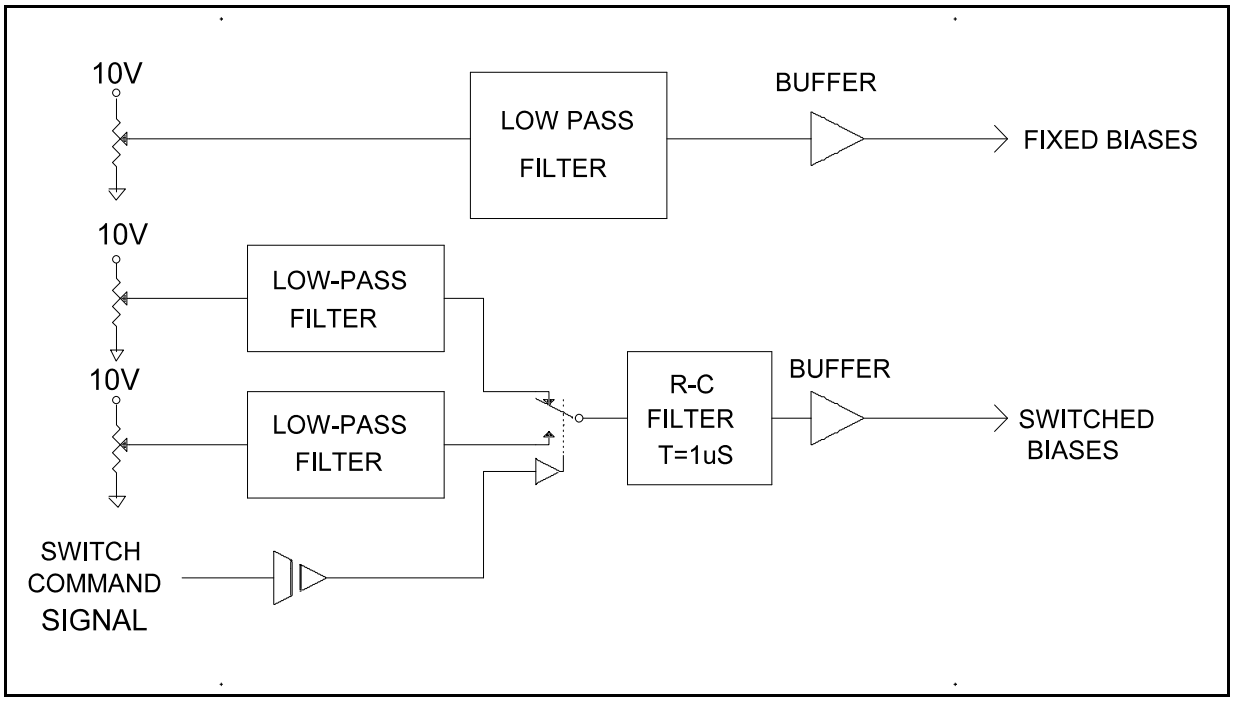

Figure 1. Bias Board Block Diagram

2.1 Grounds

The bias board has three types of ground: analog ground (AGND), digital ground (DGND), and computer ground (CGND). Analog and digital ground are separated until they connect at the bottom of the pc board near the P2 connector, in order to keep the digital transient noise from affecting the analog ground on the board. Computer ground is electrically and physically separated from the rest of the board by the ISO150 capacitive isolators. By protecting the analog and digital ground from computer ground interference, we eliminate ground loops and cross talk to the analog circuit.

2.2 Bus Connections

The Bias boards use Sun style VME bus connections (labeled P1 and P2 on the board, P2 and P3 on the backplane). Because of this bus structure, these signals are automatically connected to all the preamp boards connected to the backplane bus. The power connections come to the board from the backplane bus through P2.

2.3 Fixed Bias Voltages

The Fixed bias circuit provides the stable bias voltages needed for both detectors. The four Fixed bias voltages for the ALADDIN detector come from voltage divider circuits supplied by an AD587 +10VDC supply (U10). Because the ALADDIN detector needs negative bias voltages, the supply is inverted by an OP27 opamp (U9). The bias voltage levels are adjusted with a potentiometer accessible from the front panel (TR1 through TR6), low pass filtered (23U1 through 28U1) and then sent to the backplane bus to the bias input on the detectors. The diodes (D1 through D12) prevent the detector from receiving a positive bias voltage. The value range of each bias voltage is found in Table 1. For more information about the ALADDIN fixed biases, see NEDN 10.00.

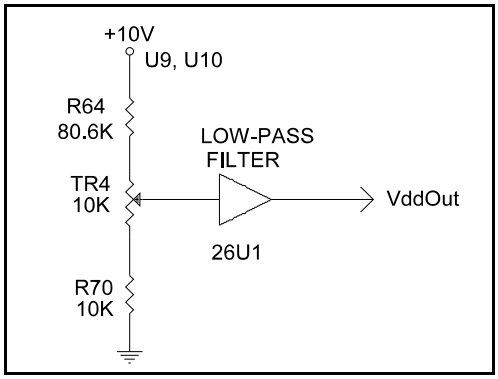

Figure 2. Fixed Bias Voltage Circuit

Table 1. ALADDIN Fixed Bias Voltages

ALADDIN Fixed Bias Signals	Board Voltage Range	Nominal Values
VssCm	-1.0 to 0.0V	0.0 V
VddOut	-1.0 to -2.0V	-1.3 V
Vref	-2.3 to 0.0V	-2.0 V
VdetCom	VddUc - VssCm	-3.0 V
VrowOff	-4.0 to 0.0V	0.0 V
VddUc	-6.0 to -3.5V	-3.8 V

2.4 Switchable Bias Voltages

The switchable bias voltages have the capacity to alternate between two different bias levels, shifting at a rate controlled by DAQ17 TTL signals. However, for our application, this switching mechanism is not used, and only one voltage level for these biases is needed. Each bias voltage level is produced on the board in the same method as the Fixed Bias voltages. They are adjusted with potentiometers (TR7 through TR12), filtered (5U1 through 16U1) and sent to the input of a pair of solid state switches (U12 through U14). The five DAQ17 digital command signals (VddCl, VggCl, VrstG, VrstR, and Vrowon) travel through ISO150 capacitive isolators (U1 through U6) to the trigger of a pair of DG201 solid state switches (U12 through U14). The TTL pulses go straight to the trigger of one switch, and the other switch has the signal inverted by a 74HC04A inverter (U19). These normally-open switches are activated by a low voltage at the trigger. Because we only need one voltage level, both of these switch circuits are set to the same voltage level. When the DAQ17 signal is TTL "high," the switch that has the inverter is activated and allows its associated voltage to travel through a low pass filter (17U1 through 22U1) to the backplane bus. The switch without the inverter turns on when the TTL clock pulse goes "low." This switching circuitry produces the switchable detector bias voltages. For more information about the ALADDIN switchable biases, see NEDN 10.00.

ALADDIN Switch Bias Signals	Nominal Values
VddCl	-3.8 V
VggCl	-1.4 V
VrstG	-3.5 V
VrstR	-2.0 V
VrowOn	-5.5 V

2.5 Summing Circuit

The summing circuit adds together two voltages, VddUc and the voltage output from the D/A Converter (U7). When the DAC (U7) receives the three command signals from the DAQ17 (CS, SCLK, and SDATA), the IC sends out a voltage, which can range from 0 to +5V. The DAC voltage is then low pass filtered (4U1), and sent to the summing circuit, as shown in Figure 4. The other voltage input to the summing circuit, VddUc, one of the fixed biases, is produced on the board from a voltage divider (TR17, R59, R60), low pass filtered (30U1), and sent to the summing circuit. An OP27 op-amp (U11) adds the two voltages at its non-inverting input. The output voltage of the op-amp, VdetCom = VddUc + DAC, is low pass filtered (29U1) and sent to the input on switch U15D, which is triggered by the latch circuit. Nominally, VdetCom = VddUc + DAC = -3.5 + 0.5 = -3.0V.

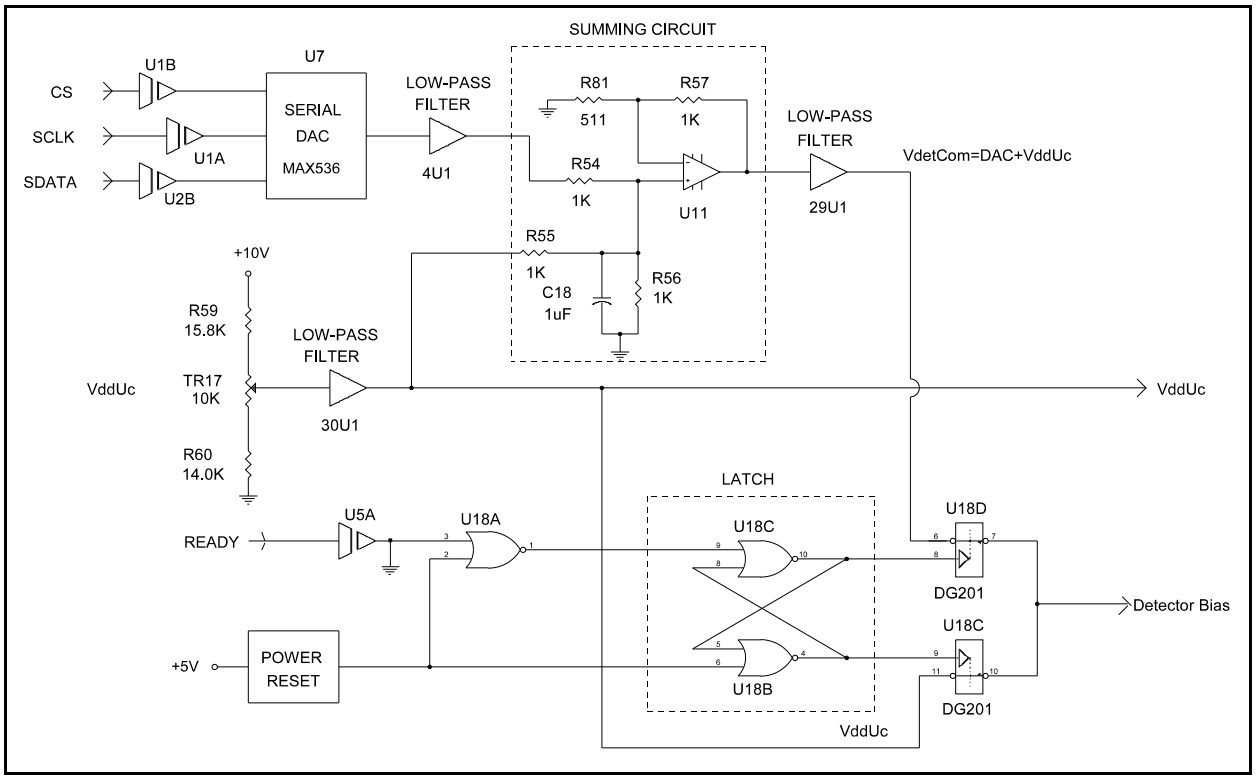

Figure 3. Latch and Summing Circuit Diagram

2.6 Latch Circuit

VdetCom switches between two voltage levels. One level is VddUc, the grounded value. The other level is Vsum, which is the biased value. The latch circuit is needed to prevent the VdetCom value switching back to Vdduc if the computer hangs up. As shown in Figure 4, the latch circuit consists of the Power Reset signal (U17), a 74HC04A NOR gate (U18A), a NOR gate latch (U18B and U18C), and two DG201 solid state switches (U15B and D). NIRSPEC does not send a ready signal from the DAQ17, so the latch is not activated. This line is connected to ground. This ground signal is routed through an ISO150 capacitive isolator (U5A) to one input of the NOR gate. The Reset signal is directed to the other NOR input. When power is first applied to the circuit, the Ready is low and the Reset signal is high, and this setup triggers the VddUc switch. After 400ms, the Reset signal goes low, and stays low unless the +5V supply to U17 is interrupted. This activates the trigger for the Vsum switch. Once VddUc goes to the Vsum value, the detector is ready.

2.7 ALADDIN Bias Board Configuration

2.7.1 Components not installed

D14
R1-R20, R55, R61
C24
J1, J4, J6, J7 through J12

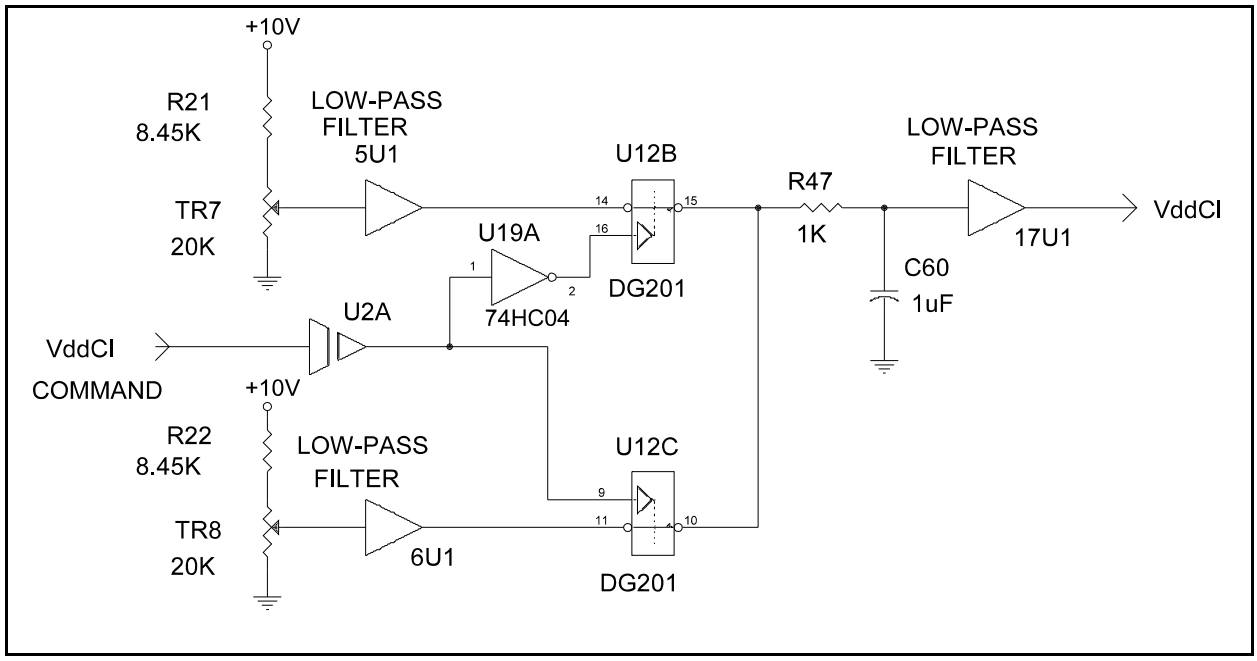

Figure 4. Switchable Bias Voltage Circuit

2.7.2 Board Modifications

Jumper wire soldered on U18 between pins 2 & 6
Jumper wire soldered on U18 between pins 4 & 8
Jumper wire soldered between U18 pin 5 & U15 pin 8
R55 end connected to C95 removed and connected to non-grounded end of R56
Soldered 1uF 20% ceramic capacitor parallel to R56
R54 end connected to TP13 removed and connected to GND
1kΩ resistor soldered between the previously vacated end of R54 and the non-grounded end of R56 (solder side of board)
Jumper added on U7 between pins 6 & 7
Jumper added on U7 between pins 13 & 14
Jumper added on U5 between pins 10 & 12

2.7.3 Jumpers Installed

J2, J3, J5

4. Functional Test Specification and Test Acceptance Procedure for ALADDIN Bias Board S/N:_____

4.1 Test Equipment Needed
Oscilloscope
Digital Multimeter
Function Generator
DC Power Supply

4.2 Drawing List
ALADDIN Bias Board Schematic: 603005
ALADDIN Bias Board Assembly Diagram: 603006

4.3 Power Supply Connection
Provide the following DC voltages and grounds to the proper pins on the board. Record the current from the power supply display.
* Power Supply for isolated computer section of board ** Static Current

Power Supply	Board Connection	Ground Connection	**Nominal Current	Measure Current
+5 ± 0.05 VDC	P2-A1	P2-C1	50 mA	mA
+15 ± 0.2 VDC	P2-C26	P2-C1	150 mA	mA
-15 ± 0.2 VDC	P2-C28	P2-C1	150 mA	mA
+5* ± 0.1 VDC	P3-6	P3-5	0.3 mA	mA

4.4 Voltage Source Verification

Measure	Description	Specification	Result
TP12 (J2 and J3 installed)	Inverted AD587 (U10) Output	-10.00±0.05VDC	VDC
TP38	AD586 (U8) Output	+5.00±0.05VDC	VDC
TP11	MC79L05 Output	-5.00±0.05VDC	VDC

4.5 Fixed Bias Circuit
This test will verify the voltage range and set the correct voltage levels of the fixed bias circuits (TR1 through TR9).

Test Conditions	Measure	Specification	Results
Adjust TR1 fully CCW.	TP39 P1-C1	0.0 ± 0.1 V	VDC
Adjust TR1 fully CW.		0.0 ± 0.1 V	VDC
Adjust TR1 so TP39 = 0.0 ±0.1V (Spare1)		0.0 ± 0.1V	VDC
Adjust TR2 fully CCW.	TP40 P1-C6	0.0 ± 0.1 V	VDC
Adjust TR2 fully CW.		-10.0 ± 0.1 V	VDC
Adjust TR2 so TP40 =-1.0 ±0.1V (Spare2)		-1.0 ± 0.1 V	VDC
Adjust TR3 fully CCW	TP41 P1-C12	0.0 ± 0.1 V	VDC
Adjust TR3 fully CW		-1.0 ±0.1 V	VDC
Adjust TR3 so TP41= 0.0±0.1V (VssCm)		0.0 ± 0.1V	VDC
Adjust TR4 fully CCW	TP42 P1-C18	-1.0 ± 0.1 V	VDC
Adjust TR4 fully CW		-2.0 ± 0.1 V	VDC
Adjust TR4 so TP42= -1.3 ± 0.1V (VddOut)		-1.3 ± 0.1V	VDC
Adjust TR5 fully CCW.	TP43 P1-C25	0.0 ± 0.1 V	VDC
Adjust TR5 fully CW.		-2.3 ± 0.1 V	VDC
Adjust TR5 so TP43 = -2.0 ±0.1V (Vref)		-2.0 ± 0.1 V	VDC

4.5 Fixed Bias Circuit (Cont.)			
Test Conditions	Measure	Specification	Results
Adjust TR6 fully CCW.	TP44 P1-C31	0.0 ± 0.1 V	VDC
Adjust TR6 fully CW.		-4.0 ± 0.1 V	VDC
Adjust TR6 so TP44 = 0.0± 0.1V (VrowOff)		0.0 ± 0.1 V	VDC
Adjust TR17 fully CCW	TP35 P2-B21	-3.5 ± 0.1 V	VDC
Adjust TR17 fully CW		-6.0 ± 0.1 V	VDC
Adjust TR17 so TP35=-3.8± 0.1V (VddUc)		-3.8 ± 0.1 V	VDC

4.6 Switchable Bias Circuit Test

4.6.1 Isolator Circuit

This test will verify that the ISO150 dual isolation buffers (U1, U2, U3, U4, U5) are transmitting digital data properly by confirming that the output signal from the buffer is of the same value and phase as the input. Apply +5V* to the isolator section by connecting +5V* at P3-6 and GND at P3-5. Send a TTL pulse (0 to +5V square wave) at f = 1.0 ± 0.1 MHz to the following inputs:

Apply 1MHz TTL Input to:	Measure	Verify
P3-1 (CS Input)	TP1	TTL?___ In Phase?___
P3-14 (SCLK)	TP2	TTL?___ In Phase?___
P3-2 (SDATA)	TP3	TTL?___ In Phase?___
P3-15 (VddCl)	TP4	TTL?___ In Phase?___
P3-3 (VggCl)	TP5	TTL?___ In Phase?___
P3-16 (VrstG)	TP6	TTL?___ In Phase?___
P3-4 (VrstR)	TP7	TTL?___ In Phase?___
P3-17 (Ready)	TP10	TTL?___ In Phase?___

4.6 Switchable Bias Circuit Test (Cont.)

4.6.2 Switchable Bias Voltage Verification

This test will verify the voltage range of the Switchable Bias Circuits (TR7 through TR16).

Test Conditions	Measure	Specification	Results
Adjust TR7 fully CCW	TP15 (High Level VddCl)	0.0 ± 0.1 VDC	VDC
Adjust TR7 fully CW		-7.0 ± 0.1 VDC	VDC
Adjust TR7 so TP15= -3.8 ± 0.1 VDC		-3.8 ± 0.1 VDC	VDC
Adjust TR8 fully CCW.	TP16 (Low Level VddCl)	0.0 ± 0.1 VDC	VDC
Adjust TR8 fully CW.		-7.0 ± 0.1 VDC	VDC
Adjust TR8 so TP16 = -3.8 ± 0.1 VDC		-3.8 ± 0.1 VDC	VDC
Adjust TR9 fully CCW.	TP17 (High Level VggCl)	0.0 ± 0.1 VDC	VDC
Adjust TR9 fully CW.		-7.0 ± 0.1 VDC	VDC
Adjust TR9 so TP17= -1.4 ± 0.1 VDC		-1.4 ± 0.1 VDC	VDC
Adjust TR10 fully CCW.	TP18 (Low Level VggCl)	0.0 ± 0.1 VDC	VDC
Adjust TR10 fully CW.		-7.0 ± 0.1 VDC	VDC
Adjust TR10 so TP18=-1.4 ± 0.1 VDC		-1.4 ± 0.1 VDC	VDC
Adjust TR11 fully CCW	TP19 (High Level VrstG)	0.0 ± 0.1 VDC	VDC
Adjust TR11 fully CW.		-7.0 ± 0.1 VDC	VDC
Adjust TR11 so TP19=-3.5 ± 0.1 VDC		-3.5 ± 0.1 VDC	VDC

4.6.2 Switchable Bias Voltage Verification (Cont.)			
Test Conditions	Measure	Specification	Results
Adjust TR12 fully CCW	TP20 (Low Level VrstG)	0.0 ± 0.1 VDC	VDC
Adjust TR12 fully CW.		-7.0 ± 0.1 VDC	VDC
Adjust TR12 so TP20= -3.5 ±0.1 VDC		-3.5 ±0.1 VDC	VDC
Adjust TR13 fully CCW	TP21, TP23 (High Level VrstR)	0.0 ± 0.1 VDC	VDC
Adjust TR13 fully CW.		-7.0 ± 0.1 VDC	VDC
Adjust TR13 so TP21=-2.0 ± 0.1 VDC		-2.0 ± 0.1 VDC	VDC
Adjust TR14 fully CCW.	TP22, TP24 (Low Level VrstR)	0.0 ± 0.1 VDC	VDC
Adjust TR14 fully CW.		-7.0 ± 0.1 VDC	VDC
Adjust TR14 so TP22= -2.0 ±0.1 VDC		-2.0 ±0.1 VDC	VDC
Adjust TR15 fully CCW.	TP25 (High Level VrowOn)	0.0 ± 0.1 VDC	VDC
Adjust TR15 fully CW.		-7.0 ± 0.1 VDC	VDC
Adjust TR15 so TP25=-5.5 ± 0.1 VDC		-5.5 ± 0.1 VDC	VDC
Adjust TR16 fully CCW.	TP26 (Low Level VrowOn)	0.0 ± 0.1 VDC	VDC
Adjust TR16 fully CW.		-7.0 ± 0.1 VDC	VDC
Adjust TR16 so TP26=-5.5 ± 0.1 VDC		-5.5 ± 0.1 VDC	VDC

4.6 Switchable Bias Circuit Test(Cont.)

4.6.3 Switchable Bias Logic Test

This test verifies that the filters (5U1 through 22U1) and the DG201 solid state switches (U12, U13, U14) are functioning properly in the Switchable Bias circuit. It also adjusts the output voltages at their correct levels. Apply +5V* to the isolator section by connecting +5V* at P1-6 and GND at P1-5. Adjust the following potentiometers to the given levels, and then apply a TTL pulse (0 to 5V square wave) at f = 65 ± 1 Hz to the corresponding P3 inputs. Verify the expected results and phase shift between the input and the output.

TTL Input	DC Voltage Levels	Measure	Results
P3-15 (VddCl)	Adjust TR7 so TP15= -3.8 ± 0.1 VDC Adjust TR8 so TP16 = -3.8 ± 0.1 VDC	TP45 P2-B5	VDC
P3-3 (VggCl)	Adjust TR9 so TP17= -1.4 ± 0.1 VDC Adjust TR10 so TP18=-1.4 ± 0.1 VDC	TP46 P2-B7	VDC
P3-16 (VrstG)	Adjust TR11 so TP19=-3.5 ± 0.1 VDC Adjust TR12 so TP20= -3.5 ±0.1 VDC	TP47 P2-B10	VDC
P3-4 (VrstR)	Adjust TR13 so TP21=-2.0 ± 0.1 VDC Adjust TR14 so TP22= -2.0 ±0.1 VDC	TP48 P2-B15	VDC
P3-7 (VrowOn)	Adjust TR15 so TP25=-5.5 ± 0.1 VDC Adjust TR16 so TP26=-5.5 ± 0.1 VDC	TP50 P2-B24	VDC

4.7 Latch Circuit Test

This test verifies the correct operation of the MAX810 reset signal generator (U17) and the 74HCT02 NOR gate (U18A) of the reset circuit. Apply +5V* to the isolator section by connecting +5V* at P3-6 and GND at P3-5. Warning: If the +5V* power supply turns off during this test, the ISO150 isolator needs to be cycled by repeating test 4.7.1.
TP36 = Reset, U18-1 = NOR gate

Test Conditions	Measure	Specification	Results
Ready = 0	TP36	+0.1± 0.2 VDC	VDC
	U18-1	+4.7± 0.3 VDC	VDC
Adjust +5V supply to +2.9± 0.2 VDC (Reset = 1)	TP36	+2.9± 0.2 VDC	VDC
	U18-1	+0.1± 0.2 VDC	VDC
Adjust +5V supply to +4.7± 0.3 VDC (Reset =0)	U18-1	+4.7± 0.3 VDC	VDC
Turn +5V supply off Measure dropoff time	TP36	Stay high for 200 ±100 msec	msec

4.8 DAC Filter Testing

This test will verify that the op-amp OP27 (4U1) circuit has a gain of ½ with J5 installed, and has a gain of -1 with J6 installed. It will also check the attenuation of the 4U1 low-pass filter circuit.

After removing the DAC (U7), apply a 2.0 ± 0.2 vP-P, f= 1.0 ± 0.1 Hz (f_0) sine-wave to U7-2, and measure V_{out} at TP13, as shown on Table 7. The circuit has a gain of ½ with J5 installed, so each V_{out} measurement should equal 1.0 vP-P and be in phase with the input voltage. With J6 installed, the circuit has a gain of -1, which will put the signal 180° out of phase with the input. The value of TP13 in this case should be 2.0 ± 0.2 vP-P and 180° out of phase with the input signal. This confirms that the op-amp circuit gain is correct.

To test the low pass attenuation, change the frequency to f = 390 ± 50 Hz, which is the 3dB point, where the output voltage should drop by a factor of -3dB, or 1/%&. Verify this attenuated voltage V_{-3dB} at TP13 for each configuration. V_{-3dB} should equal 0.7 ± 0.2 vP-P in the first configuration, and 1.4 ± 0.2 vP-P at the second configuration. The decrease in amplitude in the higher frequencies shows that the low pass filter capacitors are working properly.

*f_0= 1.0 ± 0.1 Hz **f_{-3dB} = 390 ± 50 Hz

Apply 2.0 ± 0.2 vP-P to:	Measure	Freq.	Specification	Phase	Results
U7-2	TP13 with J5 short	f_o*	1.0 ±0.2 vP-P	0°	vP-P
		f_{-3dB}**	0.7 ±0.2 vP-P		vP-P
	TP13 with J6 short	f_o	2.0 ±0.2 vP-P	180°	vP-P
		f_{-3dB}	1.4 ±0.2 vP-P		vP-P

4.9 VdetCom Circuit

This test will verify the switching mechanism between Vsum and VddUc as voltage for VdetCom.
Install J5. Remove J6 and U7 for this test.

Test Conditions	Measure	Specification	Results
Adjust TR17 so TP35 = -3.5 ± 0.1 VDC (VddUc)	TP35	-3.5 ± 0.1 VDC	VDC
Apply +1.00 ± 0.01 VDC to U7-2 (DAC Output) (Vsum = VddUc + DAC)	TP13	+0.5 ± 0.1VDC	VDC
	TP33, TP34	-3.0 ± 0.1 VDC	VDC
	U18-1	+4.7 ± 0.3 VDC	VDC
	P2-B20	-3.0 ± 0.1 VDC	VDC
Adjust +5v p.s. to +2.9 ± 0.1 VDC. (Turns reset to 1)	U18-1	+0.0 ± 0.2VDC	VDC
	P2-B20	-3.5 ± 0.1VDC	VDC