NIRSPEC

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NIRSPEC Electronics Application Note 07.00
Interface Board Description and Test Specification

1. Introduction

This document describes the performance of the interface board, and provides a functional test procedure. The interface board is the intermediary between the DAQ17 clock generator and the preamp/ADC boards. Additional information on these two boards can be found in documents NEDN 13.00 (Preamp/ADC Board) and NEDN 17.00 (DAQ17 Board). The interface board has three functions. First, it produces offset voltages that are subtracted from the detector voltage on the preamp board. By inputting three digital signals into a 12-bit serial quad D/A converter (DAC), these voltages are produced and then adjusted to a range to accommodate the detector signals. Second, the board decodes the selectable gain and filter logic signals from the DAQ17 and routes them to the gain and bandwidth circuits on the preamp boards. Third, DAQ17 Convert and Select signals are buffered and sent to the preamp A/D converter and multiplexer.

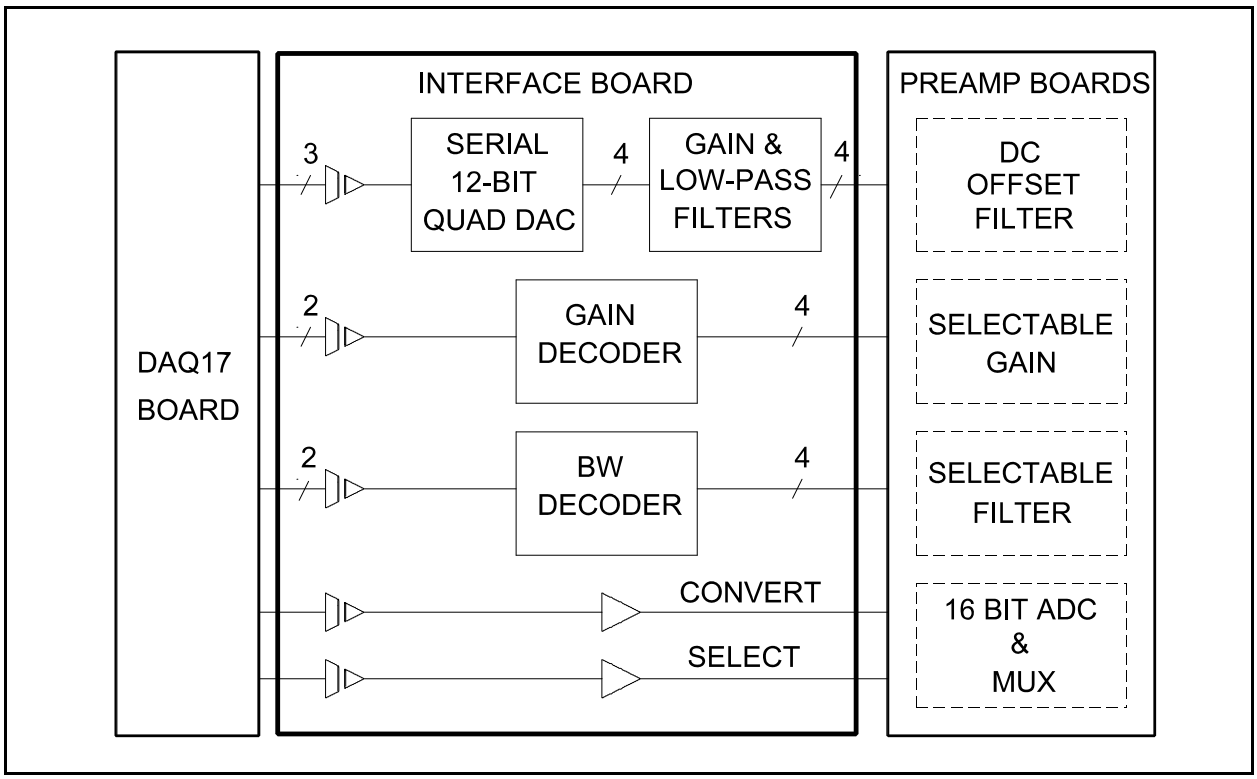


Figure 1. Interface Board Overall Block Diagram

2. General Board Description

2.1 Grounds

There are three types of ground on the interface board. The computer ground (CGND) of the DAQ17 is electrically and physically separated from the rest of the board by the ISO150 capacitive isolators. These isolators use internal capacitors to provide a high voltage barrier and to transmit digital data across this barrier. Each side of the isolator is powered by electrically separate voltage supplies. By protecting the analog ground from computer ground interference, we eliminate ground loops and cross talk to the analog circuit. The other two types of ground are analog ground (AGND) and digital ground (DGND), which are connected only at the bottom of the pc board near the P2 connector. Digital transient noise can be produced by the current fluctuations from TTL pulses, which causes the ground value to change. This ground arrangement keeps the digital noise from affecting the analog ground on the board.

2.2 Bus Connections

The Interface board uses Sun style VME bus connections (labeled “P1" and “P2" on the board, “P2" and “P3" on the backplane). Pins in rows P1-B, P2-A, and P2-C are bussed, while the other rows are not. This allows the bandwidth signals (BW0, BW1, BW2, BW3), gain signals (G0, G1, G2, G3), and offset voltages (OFFSET#1, OFFSET#2, OFFSET#3, OFFSET#4) to travel from the board through P1 to all the preamp boards connected to the backplane bus. The power connections come to the board from the backplane bus through P2.

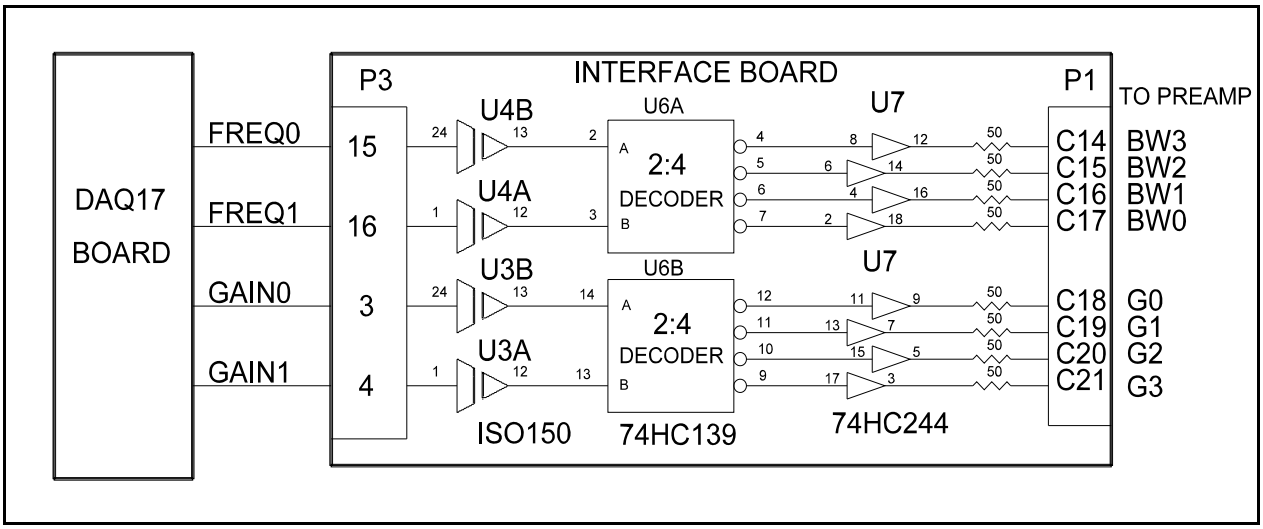


Figure 2. Selectable Gain and Filter Signal Decoder Diagram

2.3 Selectable Gain and Filter Signal Processing

Both the Gain and the Filter Signals are processed in the same manner. The DAQ17 board sends two bandwidth and two gain TTL command signals (FREQ0, FREQ1, and GAIN0, GAIN1)

to the interface board at P3, as shown on Figure 2. After passing through the ISO150 capacitive isolators U3 and U4, the signal pairs are input into a 74HC139 dual 2-of-4 decoder U6. Each decoder will generate four outputs (see Table 1), one of which will be low in order to activate a gain or filter circuit on the preamp board. The eight final decoder outputs (BW0, BW1, BW2, BW3, G0, G1, G2, and G3) are sent to a 74HC244 octal line driver U7, and then directed through the backplane bus to the selectable gain and filter circuits on the preamp/ADC boards.

Table 1. Gain and Filter Decoder Inputs and Outputs

COMMAND SIGNAL		OUTPUT SIGNAL (Active = "0")			
FREQ1 or	FREQ0 or GAIN0	BW3 or G3	BW2 or G2	BW1 or G1	BW0 or G0
0	0	1	1	1	0
0	1	1	1	0	1
1	0	1	0	1	1
1	1	0	1	1	1

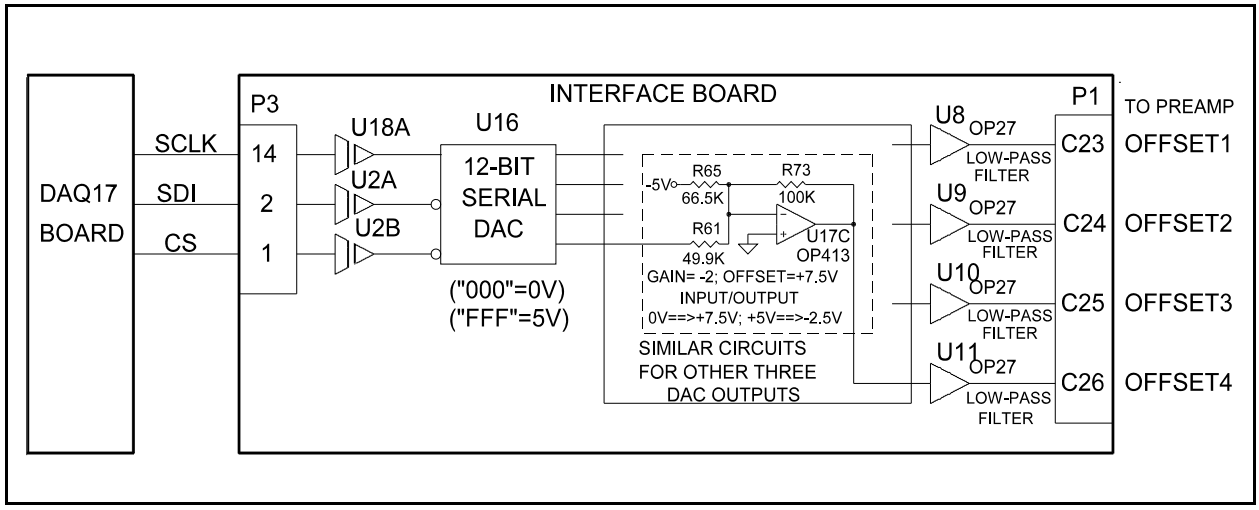
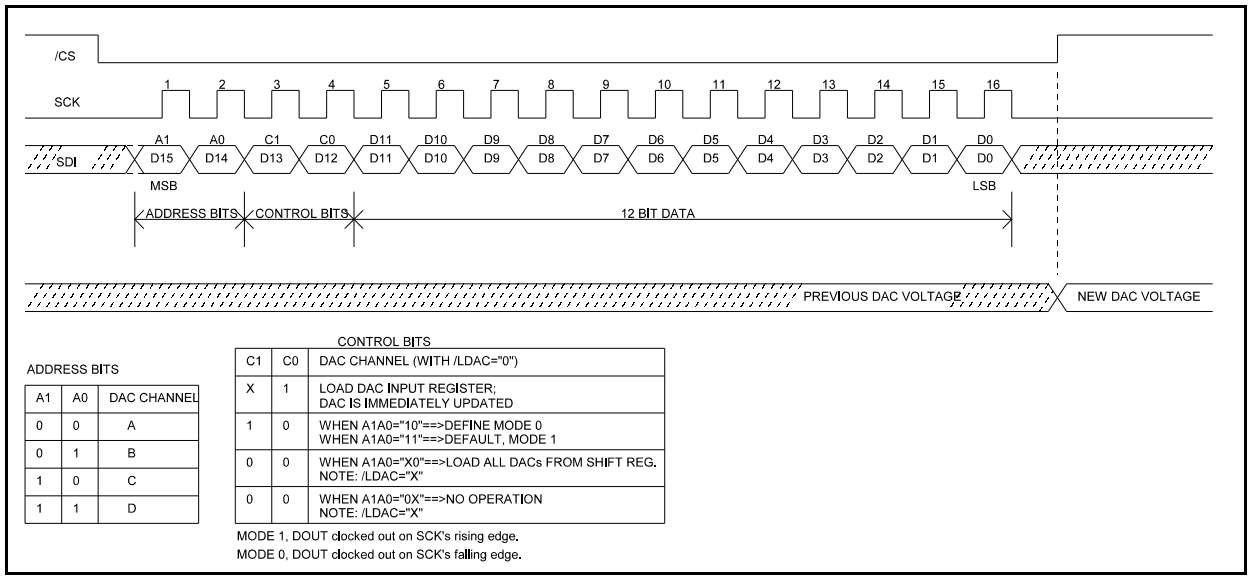


Figure 3. Offset Voltage Diagram

2.2 Offset Voltage

The offset voltages are used to subtract away detector voltages on the preamp board. Because the ALADDIN detector sends out a -2V signal and the PICNIC detector sends out a +5V signal, the interface board must produce a minimum offset range of -2V to +5V to accomodate both detectors. This is accomplished by converting DAQ17 digital signals into analog DC voltages of this required



A1	A0	DAC CHANNEL
0	0	A
0	1	B
1	0	C
1	1	D

C1	C0	DAC CHANNEL (WITH /LDAC="0")
X	1	LOAD DAC INPUT REGISTER; DAC IS IMMEDIATELY UPDATED
1	0	WHEN A1A0="10"==>DEFINE MODE 0 WHEN A1A0="11"==>DEFAULT, MODE 1
0	0	WHEN A1A0="X0"==>LOAD ALL DACs FROM SHIFT REG. NOTE: /LDAC="X"
0	0	WHEN A1A0="0X"==>NO OPERATION NOTE: /LDAC="X"

Figure 4. DAC Timing Diagram

voltage range. Three lines from the DAQ17 board, SDI (serial data in), SCLK (shift-register clock), and CS (chip select), go through ISO150 capacitive isolators U2 and U18, to the MAX536 quad 12-bit serial D/A converter (DAC) U16, as shown on Figure 3. For more information about the DAQ17 board, see NEDN 17.01. The DAC receives its -5V supply from the MC79L05 regulator U15. When the timing sequence as shown in Figure 4 is carried out, the DAC converts the hexadecimal SDI signal, with a level ranging from 000 to FFF, into one of the output DAC voltages, with a corresponding voltage of 0 to 5 VDC. The upper limit of this range is controlled by the REFAB, REFCD inputs. Each SDI input bit corresponds to 1.2 mV of DAC output voltage. The quad DAC provides four output voltages, one for each quadrant of the detector. The DAC output voltage must be adjusted to match the requirements of the detectors before it is sent to the preamp boards as offset voltage. This is accomplished with the op-amp gain circuit (U17). First, U17 amplifies the DAC output voltage by a gain of -2 using R61 and R73 (for OFFSET#4), which changes the output range to 0 to -10V. Then this range is offset by adding +7.5 VDC at the op-amp input, using a -5V input from U15 and R765 (for OFFSET#4). This converts the four DAC signals to the offset voltage range needed for both detectors, -2.5 to +7.5 VDC, as shown in Figure 5. The offset voltages are then low-pass filtered and buffered by U8, U9, U10, and U11, and sent to the offset filter on the preamp/ADC boards through the backplane bus at P1.

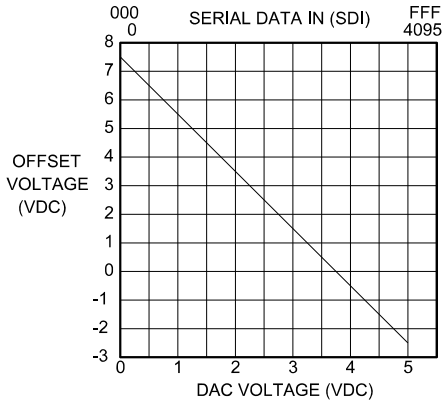


Figure 5. DAC vs Offset Voltage

2.3 ADC Control Signals

The interface board receives the A/D CONV and SELECT signals from DAQ17, as shown on Figure 6. The A/D CONV gives the command for the A/D converter in the preamp/ADC board to convert. The SELECT signal selects which channel (A or B) of the Preamp/ADC boards will be output to the data acquisition board (DAQ15). These signals are transmitted through BNC connectors to the ISO150 isolator U1 and sent through a 74HC244 buffer (U5) before they are directed to the preamp/ADC boards through the backplane bus at P1.

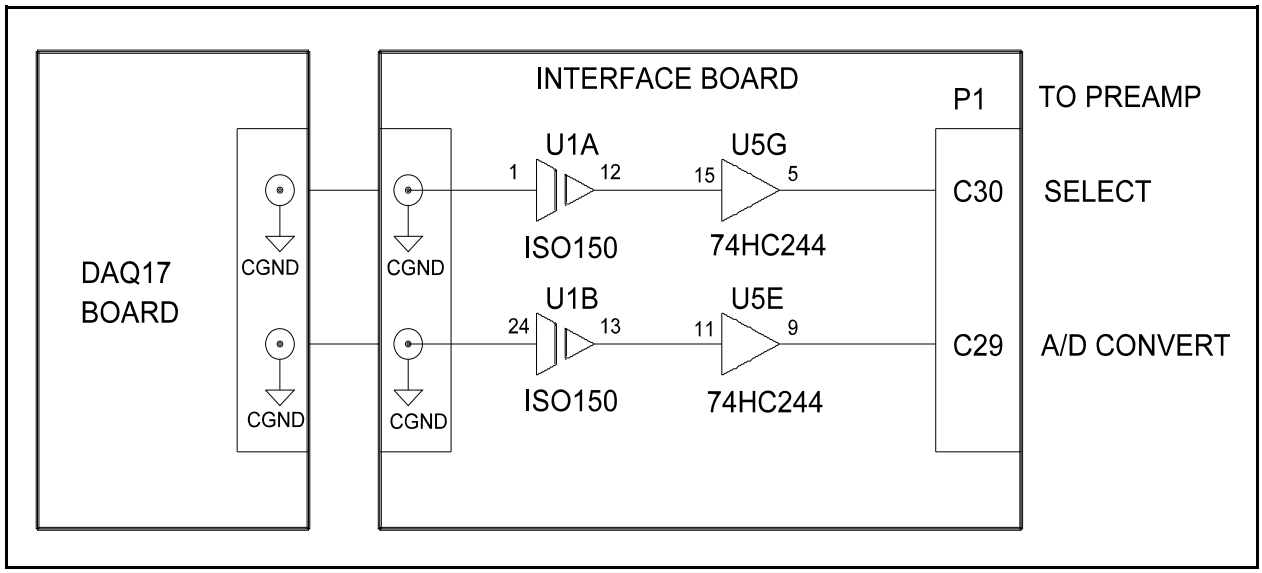


Figure 6. A/D Convert and Select Signal Processing Diagram

2.4 Interface Board Configuration

2.4.1 Components not installed

R1 - R16, R74 - R77
J1, J2, (serial numbers 1-99: J1, J2, J3, J6, J7)

2.4.2 Board Modifications

P3 track cut between pin 10 & 12 (serial numbers 100-199)

2.4.3 Jumpers Installed

J4 (serial numbers 1-99)

3. Functional Test Specification and Test Acceptance Procedure for Interface Board S/N:_____

3.1 Test Equipment Needed
Oscilloscope
Digital Multimeter
Function Generator
DC Power Supply

3.2 Drawing List
Interface Board Schematic: 603003
Interface Board Assembly Drawing: 603004

3.3 Power Supply Connection
Provide the following DC voltages and grounds to the proper pins on the board. Record the power supply current from its display.
* Power Supply for isolated computer section of board ** Static Current

Power Supply	Board Connection	Ground Connection	**Nominal Current	Measured Current
+5 ± 0.05 VDC	P2-A1	P2-C1	40 mA	mA
+15 ± 0.2 VDC	P2-C26	P2-C2	35 mA	mA
-15 ± 0.2 VDC	P2-C28	P2-C3	30 mA	mA
+5* ± 0.1 VDC	P3-25	P3-24	1 mA	mA

3.4 Voltage Source Verification

Measure	Description	Specification	Result
TP16	AD586 (U14) Output	+5.00 ± 0.05 VDC	VDC
TP15 (with J5 installed)	Inverted AD586 (U14) Output	-5.00 ± 0.05 VDC	VDC
U16-3	MC79L05 (U15) Output	-5.0 ± 0.1 VDC	VDC

3.5 Offset Voltage Range Verification

This test will verify that the voltage range of each offset output is -2.5V to +7.5V, when 0 to +5 VDC is applied to the op-amp from the D/A converter (U16). After U16 has been removed, apply an input DC voltage of +5V to each of the following U16 pins, and measure the output voltages at the given pins. Verify the predicted voltage of -2.5V. Change the input voltages to 0V. Measure the output voltages again to confirm a +7.5V result.

DC Voltage Input	Measure	Specification	Result
U16-2 =+5V	U17-8	-2.5 ± 0.2 VDC	VDC
U16-2 = 0V		+7.5 ± 0.2 VDC	VDC
U16-1 = +5V	U17-14	-2.5 ± 0.2 VDC	VDC
U16-1 = 0V		+7.5 ± 0.2 VDC	VDC
U16-16 = +5V	U17-1	-2.5 ± 0.2 VDC	VDC
U16-16 = 0V		+7.5 ± 0.2 VDC	VDC
U16-15 = +5V	U17-7	-2.5 ± 0.2 VDC	VDC
U16-15 = 0V		+7.5 ± 0.2 VDC	VDC

3.6 Isolator Circuit

This test will verify that the ISO150 dual isolation buffers (U1, U2, U3, U4, U18) are transmitting digital data properly by confirming that the output signal from the buffer is of the same value and phase as the input. Apply +5V* to the isolator section by connecting +5V* at P3-25 and GND at P3-24. Send a TTL pulse (0 to 5 V square wave) at f = 1.0 ± 0.1 MHZ to the following inputs:

Apply 1MHz TTL Input to:	Measure	Verify
A/D CONV (BNC)	TP1, P1-C29	TTL?___ In Phase?___
SELECT (BNC)	TP2, P1-C30	TTL?___ In Phase?___
FREQ0 (P3-15)	TP22	TTL?___ In Phase?___
FREQ1 (P3-16)	TP6	TTL?___ In Phase?___
GAIN0 (P3-3)	TP5	TTL?___ In Phase?___
GAIN1 (P3-4)	TP21	TTL?___ In Phase?___
CS (P3-1)	TP3, U16-9	TTL?___ In Phase?___
SDI (P3-2)	TP4, U16-8	TTL?___ In Phase?___
SPARE (P3-17)	U18-13	TTL?___ In Phase?___
SCLK (P3-14)	U16-10	TTL?___ In Phase?___

3.7 Logic Decoder Circuit

This test will verify that the 74HC139 dual decoder (U6) is decoding properly, and the 74HC244 octal line driver (U7) is buffering the signals. Make sure that +5V* is applied to Isolator Section, i.e. P3-25 (+5V*) & P3-24 (CGND). Apply a TTL (0 to 5 V square wave) at f = 1.0 ± 0.1 kHz square wave to each of the following TTL Inputs, and apply the given DC Logic Level to the stated locations. Verify the expected results..

1kHz TTL Input	DC Input	Measure	Specification	Results
P3-15 (FREQ0)	Connect TP6 to GND	TP11 &R21	TTL(phase= 0°)	Hi:____/Lo___V
		TP12 & R22	TTL(phase=180°)	Hi:____/Lo___V
		TP13 & R23	"1"	V
		TP14 & R24	"1"	V
P3-15 (FREQ0)	Connect TP6 to TP16 (5V)	TP11 & R21	"1"	V
		TP12 & R22	"1"	V
		TP13 & R23	TTL(phase= 0°)	Hi:____/Lo___V
		TP14 & R24	TTL(phase=180°)	Hi:____/Lo___V
P3-3 (GAIN0).	Connect TP21 to GND	TP10 & R25	TTL(phase= 0°)	Hi:____/Lo___V
		TP9 & R26	TTL(phase=180°)	Hi:____/Lo___V
		TP8 & R27	"1"	V
		TP7 & R28	"1"	V
P3-3 (GAIN0).	Connect TP21 to TP16 (5V)	TP10 & R25	"1"	V
		TP9 & R26	"1"	V
		TP8 & R27	TTL(phase= 0°)	Hi:____/Lo___V
		TP7 &R28	TTL(phase=180°)	Hi:____/Lo___V

3.8 DAC Filter Testing

This test will verify that the op-amp OP413FP (U17) circuit has a gain of -2, and will also check the attenuation of the low-pass filters (U8-U11). Apply a 2.0 ± 0.2 vP-P, f = 0.1 ± 0.01 Hz (f_0) sine-wave to each of the following U16 pins, and measure V_{out} at the corresponding U17 and P1 pins. The circuit has a gain of -2, which will invert and double the amplitude of the input sine wave, so each V_{out} measurement should equal 4.0 vP-P and be 180° out of phase with the input voltage. This confirms that the op-amp circuit gain is correct. To test the low pass attenuation, change the frequency to f = 2.0 ± 0.2 Hz. This frequency is the 3dB point, where the output voltage should drop by a factor of -3dB, or 1/%&. Verify this attenuated voltage at each output point for all four filters, which will equal 3.0 ± 0.2 vP-P at the first filter (U17) output, and 2.0 ± 0.2 vP-P at the second filter (P1) output. The decrease in amplitude shows that the low pass filter capacitors are working properly. **f_0= 0.1 ± 0.01 Hz *f_{-3dB} = 2.0 ± 0.2 Hz

Apply 2.0 ± 0.2 vP-P to:	Freq.	Measure	Specification		Result
			Value	Phase	
U16-2	f_o**	U17-8 & OFFSET#1	4.0 ±0.2 vP-P	180°	vP-P
	f_{-3dB}*	U17-8	3.0 ±0.2 vP-P	180°	vP-P
		OFFSET#1	2.0 ±0.2 vP-P	180°	vP-P
U16-1	f_o	U17-14 & OFFSET#2	4.0 ±0.2 vP-P	180°	vP-P
	f_{-3dB}	U17-14	3.0 ±0.2 vP-P	180°	vP-P
		OFFSET#2	2.0 ±0.2 vP-P	180°	vP-P
U16-16	f_o	U17-1 & OFFSET#3	4.0 ±0.2 vP-P	180°	vP-P
	f_{-3dB}	U17-1	3.0 ±0.2 vP-P	180°	vP-P
		OFFSET#3	2.0 ±0.2 vP-P	180°	vP-P
U16-15	f_o	U17-7 & OFFSET#4	4.0 ±0.2 vP-P	180°	vP-P
	f_{-3dB}	U17-7	3.0 ±0.2 vP-P	180°	vP-P
		OFFSET#4	2.0 ±0.2 vP-P	180°	vP-P