NIRSPEC

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NIRSPEC Electronics Application Note 06.00
Preamp/ADC Board Test Specification

1. Introduction

` This document describes the functional and performance test specifications for the preamp/ADC board. Figure 1 is the block diagram showing the input/output signals of the preamp/ADC board. The offset circuits subtract the offset from the detector array. The preamplifier circuit amplifies the low level signal, and supplies a constant load current to the array. The selectable gain circuit determines the amount of gain added to the signal, and the selectable frequency circuit determines the range of low pass filtering done on the signal. The analog signal is converted to digital through the ADC, and then multiplexed and sent to the DAQ15 board. Throughout this document, channel 1 will be described only, because channel 2 is identical except the reference number destination. To get the reference number destination for channel 2, add 1 to reference destination for channel 1.

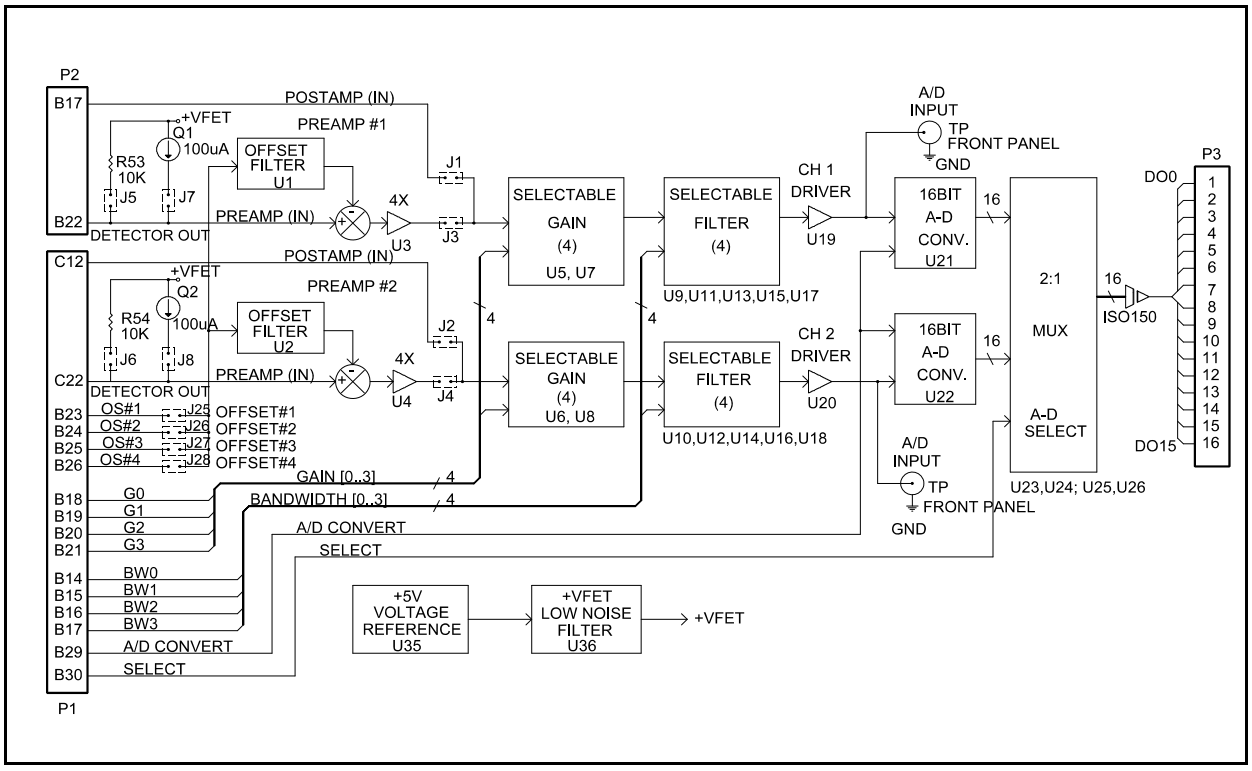

Figure 11. Preamp Board Functional Block Diagram

2. General Description

2.1 Grounds

The preamp board has three types of ground: analog ground (AGND), digital ground (DGND), and computer ground (CGND). Analog and digital ground are separated until they connect at the bottom of the pc board near the P2 connector, in order to keep the digital transient noise from affecting the analog ground on the board. Computer ground is electrically and physically separated from the rest of the board by the ISO150 capacitive isolators. By protecting the analog and digital ground from computer ground interference, we eliminate ground loops and cross talk to the analog circuit.

2.2 Bus Connections

The Preamp boards use Sun style VME bus connections (labeled P1 and P2 on the board, P2 and P3 on the backplane). Pins in rows P1-B, P2-A, and P2-C are bussed, while the other rows are not. Because of this bus structure, signals in the bussed pins (bandwidth signals, gain signals, and offset voltages from the Interface Board) are automatically connected to all the Preamp boards through the backplane bus. The power connections come to the board from the backplane bus through P2.

2.3 JFET Bias Circuit

The purpose of this circuit is to provide an ultra low noise bias voltage to the constant current FET Q1 or the load resistor R53, depending on the board setup. Figure 2 shows the +Vfet bias source circuit. The +Vfet circuit is composed of two parts, the +5.0VDC voltage reference U35 and a low pass filter U36. The reference voltage from U35 is sent to a voltage divider, which determines the value of the Vfet voltage. As shown in Figure 2, +Vfet = +5v[R84/(R83+R84)]= +4.0VDC. The Vfet voltage is then sent to the low pass filter U36, and then to the Preamp Circuit at FET Q1.

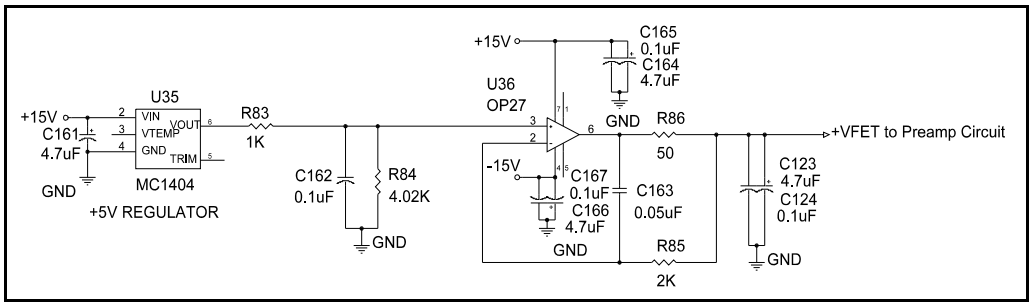

Figure 2. JFET Bias Circuit Diagram

2.4 Preamplifier Circuit

The purpose of the preamplifier circuit is to supply either a constant load current or a constant voltage source to the detector array, to subtract the dc offset from the detector array, and to amplify the low level detector signal. This circuit is shown in Figure 3.

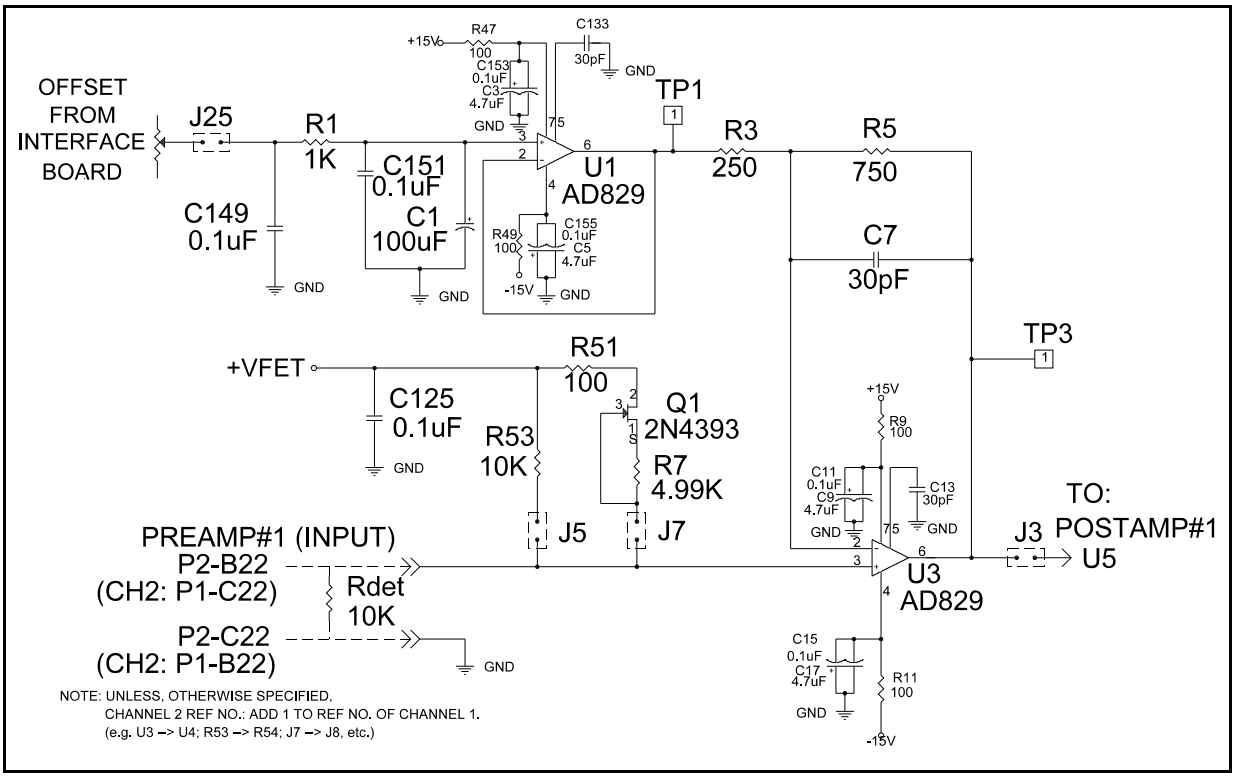

Figure 3. Preamplifier Circuit

2.4.1 FET Circuit

The purpose of this circuit is to add a constant current or voltage source to the detector array before it is amplified. In order to have a constant voltage source, J5 is installed, so that the Vfet voltage is sent through R53 to the detector array, as shown in Figure 3. In order to have a constant current source, J7 is installed, and the Vfet voltage is sent through R51, Q1, and R7. The 2N4393 FET Q1 is a stable low noise current source, and with J7 installed, this current is sent to the detector array.

2.4.2 Offset Circuit

The purpose of the offset circuit is to remove the dc offset from the detector array output. The amount of offset required is proportional to the load current and the detector array impedance. The adjustable offset voltage comes from the Interface board (NEDN 14.00), and is fed into a low noise filter, U1. As shown in figure 3, the output of this filter is sent to one input of opamp U3, which subtracts the offset voltage from the detector signal. The postamplifier (U5), will further amplify the IR signal from the preamplifier output.

The layout of the offset voltage on the ALADDIN preamp board differs from that of the PICNIC preamp board. For the ALADDIN detector, each quadrant of data is made up of four preamp boards, with a total of eight channels per quadrant. On the other hand, each quadrant of the PICNIC detector is made up of one channel from a board. This means that the on the ALADDIN preamp board, each channel will get the same offset voltage from the Interface board, since both of

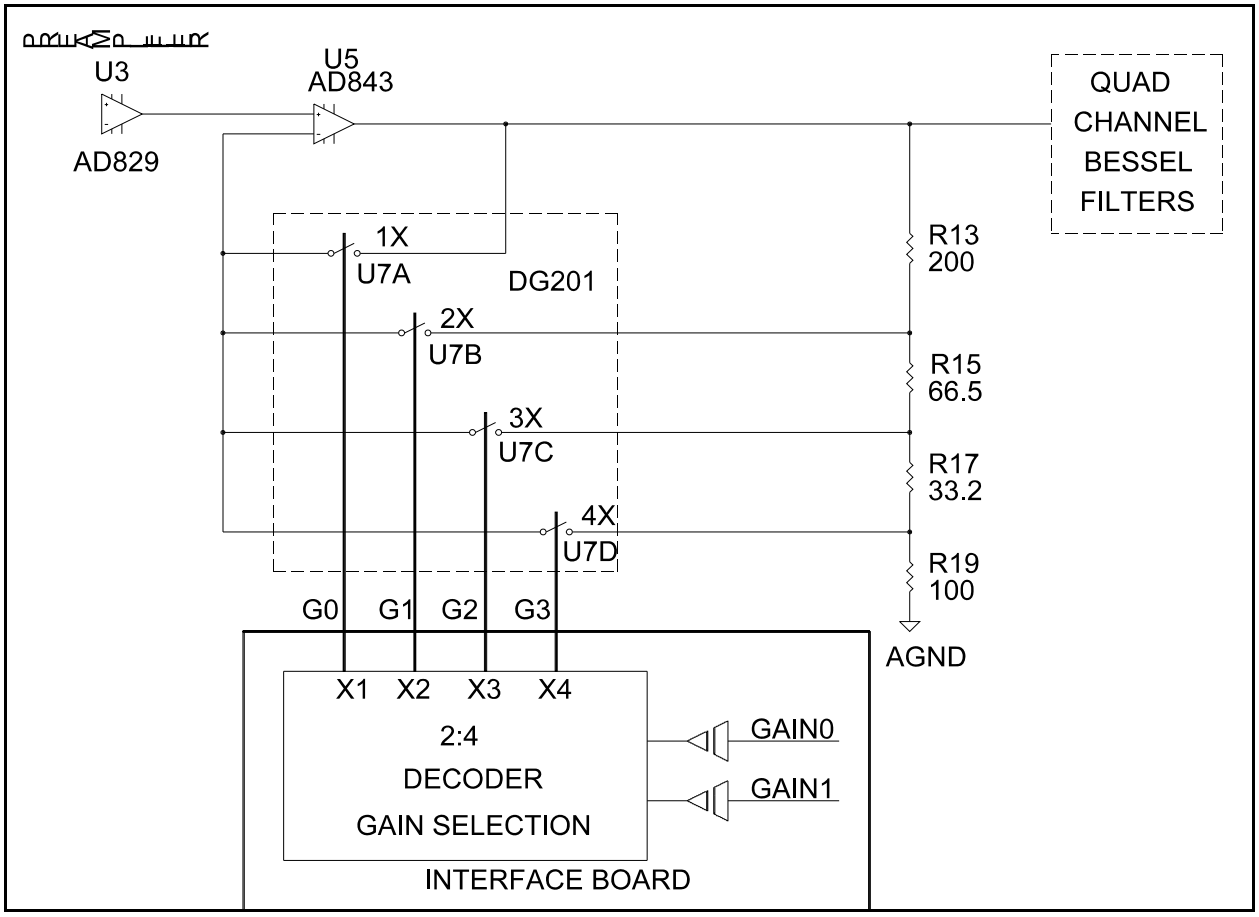

Figure 4. Selectable Gain Circuit Diagram (Channel 1)

them contribute to the same quadrant. However, each channel on the PICNIC preamp board will get individual offset voltages from the Interface board, because each channel represents a separate quadrant. Therefore, on the ALADDIN preamp board, the offset voltage for both channels are physically tied together, while the PICNIC preamp board has individual offset voltage lines for each channel. This is achieved either from different board layouts for boards with serial numbers 000 to 099, or by the installation or removal of J24 for boards with serial numbers 100 to 199.

2.5 Selectable Gain / Postamplifier Circuit

The optimum location for the selectable gain circuit is after the preamplifier. This will maximize the signal level before the A/D converter. With the higher signal, the susceptibility to noise pickup will be greatly reduced. Figure 4 shows the selectable gain circuit. This postamplifier (U5 & U7) consists of four selectable gain switch circuits. The gain is set by the analog switch (U7) and the resistor ladder network (R13, R15, R17, and R19). As shown in Table 1, gain is set by turning on U7 switches by the input of the appropriate code from the Interface board. When a switch is activated, it completes a specific gain circuit on the preamp. The signal is then sent to the Selectable Filter Circuit.

TABLE 1 Postamplifier Gain Table

Setting	Gain Code $G_0\ G_1\ G_2\ G_3$	Activated Switch	Gain Value
1	0 1 1 1	U7A	1
2	1 0 1 1	U7B	2
3	1 1 0 1	U7C	3
4	1 1 1 0	U7D	4

2.6 Selectable Bandwidth Circuit

The commonly used "3-dB" signal bandwidth (f_{-3dB}) is defined as the frequency of the half-power point. A 3-dB reduction represents a loss of 50% in power level and corresponds to a voltage level equal to 1/%& of the voltage at the reference. Figure 6 shows a unity gain Sallen-Key low pass filter circuit. The low pass filter consists of four independent selectable unity gain filters, as shown in Figure 5. The bandwidth of each filter is determined by two resistors and two capacitors, for example U9 has R25, C27, R27, and C29. The detector signal comes from the Postamplifier U5 to

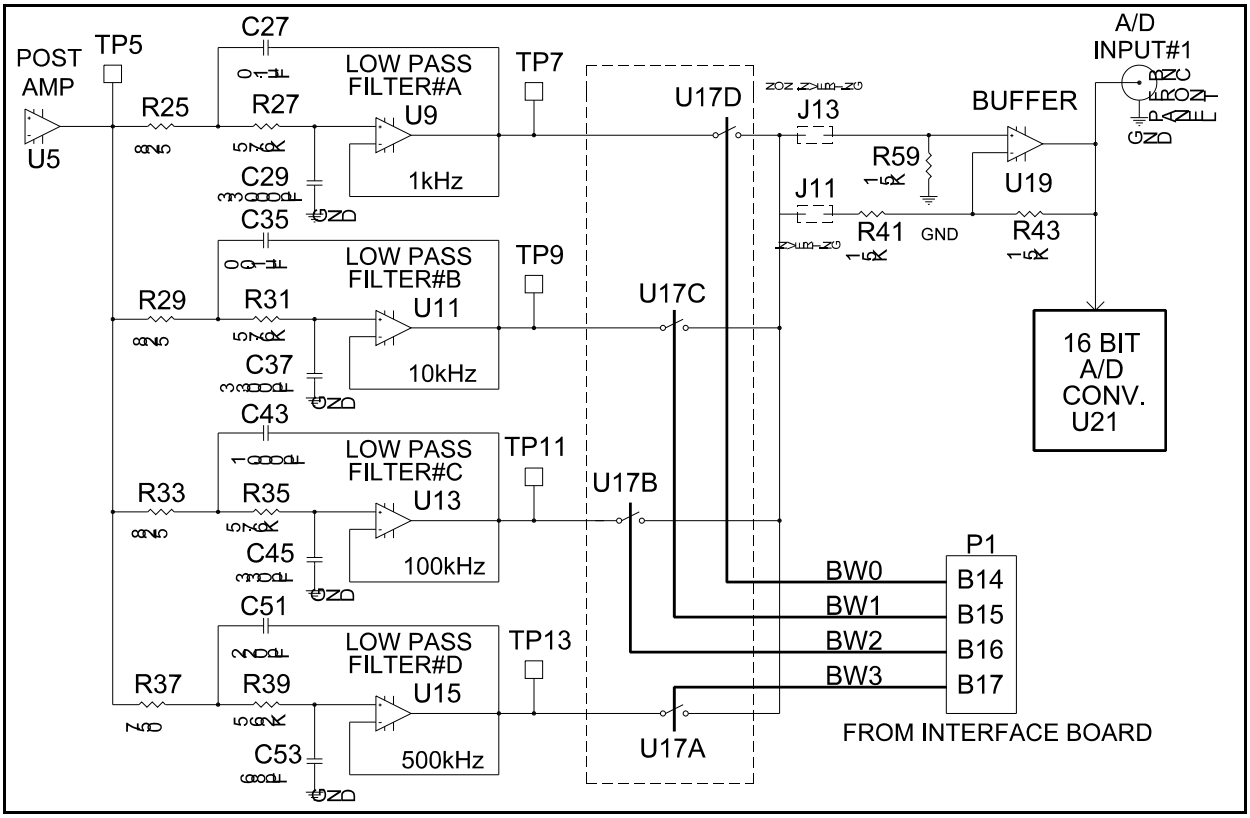

Figure 5. Low Pass Sallen-Key Bessel Filter Diagram (Channel 1)

each of the four low pass filter circuits (U9 through U16). A switch (U17) connects the output of the filters to the A/D input. The trigger pulses for the switches come from the Interface board through P1. Table 2 shows the command codes for activating each switch. When a switch is activated, it sends its filtered signal through the driver U19 to the A/D Input U21 through either J11 or J13. J11 is used to invert the signal through the buffer for the ALADDIN board. J13 is non-inverting for PICNIC detector signals.

Table 2 BW Code for Low Pass Filter Selection

Bandwidth Code	Input Pin	Bandwidth
BW_3	P1-B17	500KHz
BW_2	P1-B16	100KHz
BW_1	P1-B15	10KHz
BW_0	P1-B14	1KHz

2.7 Analog to Digital Conversion and Multiplexing Circuit

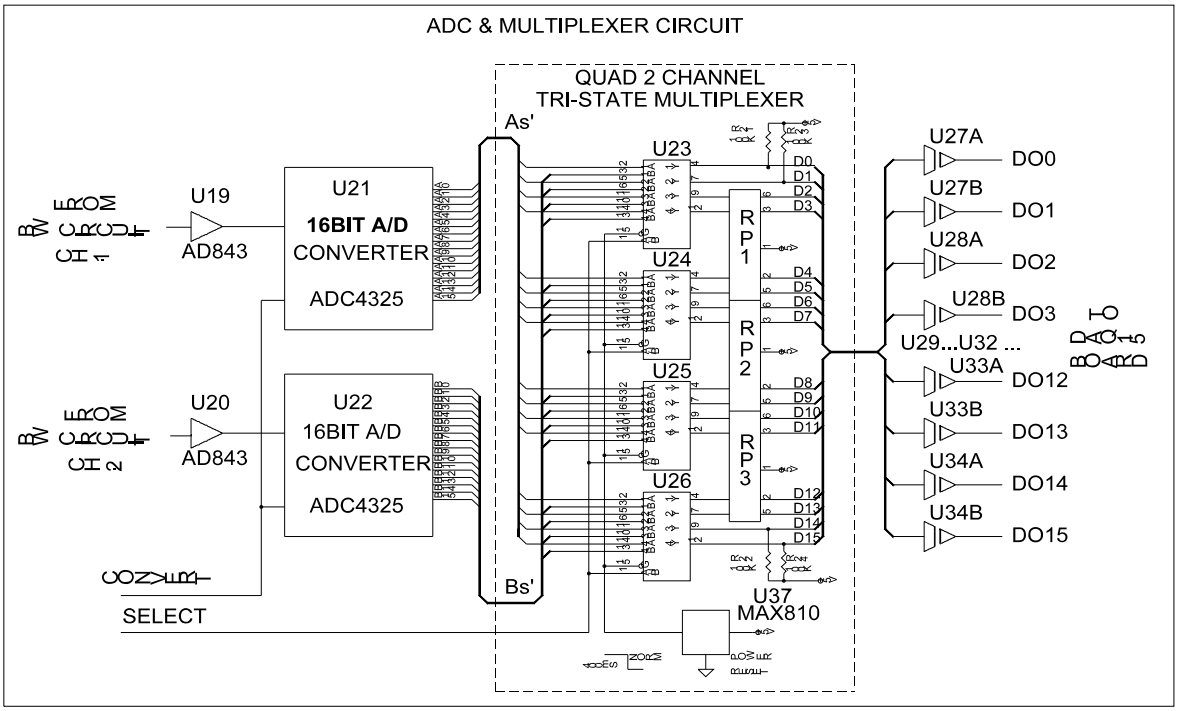

Figure 6. ADC and Multiplexer Circuit Diagram

The detector signal is sent to the 16 bit ADC4325 A/D Converters U21and U22, one for each channel. When the IC receives a negative-edged A/D CONV pulse from the Interface board at the trigger input (pin 19), the ADC converts the analog voltage into a 16 bit digital signal.

The outputs from the ADC are then sent to four 74HCT157 multiplexers U23, U24, U25, and U26. This is necessary in order to combine the 16 bit data from both channels into one bus of 16 lines. The multiplexing is controlled by the SELECT pulse from the Interface board, which chooses which multiplexer to activate by the level of the SELECT signal (high activates channel 1, low activates channel 2 on all multiplexers). This process routes the data from the two ADC through the four multiplexers and the ISO 150 isolators (U27A through U34B) to the DAQ15 board. The MAX810 reset circuit U37 is needed to reset the ISO150 isolators before data is transferred, so that they transmit correct information.

2.8 1024 Preamp Board Configuration

2.8.1 Components not installed

C7, C8, C135, C136, C143, C144
TR1, TR2
J1, J2, J5, J6, J9, J10, J11, J12, J17, J18, J19, J20, J25, J26, J27, J28, J29

2.8.2 Board Modifications

Jumper wire from P1-C27 to common junction of J25, J26, J27, J28

2.8.3 Jumpers Installed

J3, J4, J7, J8, J13, J14, J15, J16, J21, J22, J24(serial numbers 100-199)

2.9 256 Preamp Board Configuration

2.9.1 Components not installed

C7, C8, C135, C136, C143, C144
TR1, TR2
J1, J2, J7, J8, J9, J10, J13, J14, J17, J18, J19, J20, J24(serial numbers 100-199), J25, J26, J27, J28, J29

2.9.2 Board Modifications (for all serial numbers)

Jumper wire from P1-C27 to common junction of J25, J26, J27, J28
Remove non-grounded end of C150 and connecting end of R2, reconnect them out of board
Connect a jumper from the floating junction of C150 and R2 to the non-grounded end of R46

2.9.3 Jumpers Installed

J3, J4, J5, J6, J11, J12, J15, J16, J20, J21

3. Functional Test Specification and Test Acceptance Procedure for the Preamp/ADC Board S/N:_____

3.1 Test Equipment Needed

Oscilloscope
Digital Multimeter
Function Generator
DC Power Supply

3.2 Drawing List

Preamp/ADC Board Schematic: 603001
Preamp/ADC Board Assembly Diagram: 603002

3.3 Power Supply Connection

Provide the following DC voltages and grounds to the proper pins on the board. Record the current from each power supply.
* Power Supply for isolated computer section of board ** Static Current

Power Supply	Board Connection	Ground Connection	**Nominal Current	Measure Current
+5 ± 0.05 VDC	P2-A1	P2-C1	10 mA	mA
+15 ± 0.2 VDC	P2-C26	P2-C1	200 mA	mA
-15 ± 0.2 VDC	P2-C28	P2-C1	250 mA	mA
+5* ± 0.1 VDC	P3-17	P3-20	50 mA	mA

3.4 VFET Voltage Source Verification

This tests verifies the VFET circuit output.

Measure	Specification	Result
J29-2	+4.00 ± 0.05 VDC	VDC

3.5 Detector Bias Voltage Source

This test verifies that the constant voltage source will be provided to the preamp when J5 and J6 are installed. A 10K resistor is connected from P2-B22 or U3-3 or U3-3 and P2-C22 or U4-3 to Gnd. This creates a voltage divider (R53 and added resistor, R54 and added resistor) which divides the VFET voltage in two.

Install J5 and J6. Remove J7 and J8.

Setup (Test Conditions)	Measure	Specification	Result
Terminate P2-B22 (or U3-3) with 10K to Gnd.	P2-B22 (U3-3)	+2.0 ± 0.1VDC	v
Terminate P1-C22 (or U4-3) with 10K to Gnd.	P1-C22 (U4-3)	+2.0 ± 0.1VDC	v

3.6 Detector Bias Current Source

This test verifies that the constant current source will be provided to the preamp when J7 and J8 are installed. A 1K resistor is connected from P2-B22 or U3-3 and P2-C22 or U4-3 to Gnd. This provides a resistance across which one can measure the voltage to verify the correct current value.

Install J7 and J8. Remove J5 and J6.

Setup (Test Conditions)	Measure	Specification	Result
Terminate P2-B22 (or U3-3) with 1.00K to Gnd	P2-B22 (U3-3)	+240 ± 10mVDC	mv
Terminate P1-C22 (or U4-3) with 1.00K to Gnd.	P1-C22 (U4-3)	+240 ± 10mVDC	mv

3.7 Offset Circuit

3.7.1 Buffer Test

This test verifies the operation of the buffers U1 and U2.
Install J24 and J25. Remove J5, J6, J7, J8. Apply +5.0 ± 0.1VDC to P2-B23.

Measure	Specification	Result
TP1	+5.0 ± 0.1VDC	VDC
TP2	+5.0 ± 0.1VDC	VDC

3.7 Offset Circuit

3.7.2 DecayTime Constant

This test measures the rising and falling time constant (90% to 10%) for the opamps U1 and U2 when supply voltage is turned off and on.

Conditions (Test Setup)	Measure	Specification	Result
Turn off +5V supply to P2-B23 to measure falling time constant.	TP1	>90ms	ms
	TP2		ms
Turn on +5V supply to P2-B23 to measure rising time constant.	TP1	>90ms	ms
	TP2		ms

3.8 Preamp Circuit

3.8.1 Gain and Frequency Test

This test verifies the gain and frequency responses from the preamp circuit.
Apply a 250± 25mVp-p, 1.0± 0.1kHz sine wave to Preamp Input at P2-B22 or J7-2 (ch.1) or P1-C22 or J6-2 (ch.2). Connect P1-B23 with J25 installed or J25-2 to GND. Measure the voltage gain and frequency response at TP3 and TP4 using a scope, sync to an external source. Adjust the frequency of the input voltage to determine the f_{-3dB} for the circuit. (f_{-3dB} occurs when the voltage decreases to 1/%& of original frequency, i.e. from 4 div to 2.8div or 5div to 3.5div. on the scope)

Measure	Specification	Result
TP3 with sinewave at P2-B22 or J7-2	1.0±0.1vP-P	V
TP4 with sinewave at P1-C22 or J6-2	1.0±0.1vP-P	V
f_{-3dB} at TP3 (ch.1)	Must be > 15 Mhz	Greater than 15 MHz?_____
f_{-3dB} at TP4 (ch.2)	Must be > 15 Mhz	Greater than 15 MHz?_____

3.8 Preamp Circuit

3.8.2 Pulse Response Test

This test measures the amount of voltage "spike" that the opamp produces when input with a square wave.
Apply a 250±25mVp-p, 500±10kHz square wave to Preamp Input - Ch1 at P2-B22 (J7-2 or J5-2) or Preamp Input - Ch. 2 at P1-C22 (J8-2 or J6-2). Measure the pulse response at output of Preamp with a scope sync to external source.

Test Setup	Measure	Specification	Result
Apply 250±25mVp-p square wave to Preamp Input - Ch1 at P2-B22	TP3 spike voltage	<100mV	mV
Apply 250±25mVp-p square wave to Preamp Input - Ch. 2 at P1-C22	TP4 spike voltage	<100mV	mV

3.9 Postamp Circuit

3.9.1 Gain Test

This procedure tests each gain circuit for proper voltage amplification for each channel.
Install shorting jumpers to J3 & J4. Apply a 250 ± 25mVp-p, 1.0 ± 0.1kHz sine wave to Preamp In Ch. 1 at P2-B22 (J7-2 or J5-2) or Preamp In Ch. 2 at P1-C22 (or J8-2 or J6-2)

Circuit	Test Setup	Measure	Specification	Result
G=1 (Channel 1)	Connect P1-B18 (or U7-1) to GND Connect P1-B19 (or U7-16), P1-B20 (or U7-8), P1-B21 (or U7-9) to +5V	TP5	1.0 ± 0.1 Vp-p	Vp-p
G=1 (Channel 2)	Connect P1-B18 (or U8-1) to GND Connect P1-B19 (or U8-16), P1-B20 (or U8-8), P1-B21 (or U8-9) to +5V	TP6	1.0 ± 0.1 Vp-p	Vp-p
G=2 (Channel 1)	Connect P1-B19 (or U7-16) to GND Connect P1-B18 (or U7-1), P1-B20 (or U7-8), P1-B21 (or U7-9) to +5V	TP5	2.0 ± 0.2 Vp-p	Vp-p
G=2 (Channel 2)	Connect P1-B19 (or U8-16) to GND Connect P1-B18 (or U8-1), P1-B20 (or U8-8), P1-B21 (or U8-9) to +5V	TP6	2.0 ± 0.2 Vp-p	Vp-p
G=3 (Channel 1)	Connect P1-B20 (or U7-9) to GND Connect P1-B18 (or U7-1), P1-B19 (or U7-16), P1-B21 (or U7-8) to +5V	TP5	3.0 ± 0.3 Vp-p	Vp-p
G=3 (Channel 2)	Connect P1-B20 (or U8-9) to GND Connect P1-B18 (or U8-1), P1-B19 (or U8-16), P1-B21 (or U8-8) to +5V	TP6	3.0 ± 0.3 Vp-p	Vp-p
G=4 (Channel 1)	Connect P1-B21 (or U7-8) to GND Connect P1-B18 (or U7-1), P1-B19 (or U7-16), P1-B20 (or U7-9) to +5V	TP5	4.0 ± 0.4 Vp-p	Vp-p
G=4 (Channel 2)	Connect P1-B21 (or U8-8) to GND Connect P1-B18 (or U8-1), P1-B19 (or U8-16), P1-B20 (or U8-9) to +5V	TP6	4.0 ± 0.4 Vp-p	Vp-p

3.10 Low Pass Bessel Filter Circuit

This test verifies the f_{-3dB} for each of the filter circuits.

Remove J1 and install it to J3. Remove J2 and install it to J4. Set Postamp gain to 1 by connecting P1-B18 (or U7-1) to GND and P1-B19 (or U7-16), P1-B20 (or U7-8), P1-B21 (or U7-9) to +5V for channel 1. For Postamp Gain =1 Channel 2, connect P1-B18 (or U8-1) to GND, and P1-B19 (or U8-16), P1-B20 (or U8-8), P1-B21 (or U8-9) to +5V.

Apply a 250±25mVp-p, 1.0±0.1kHz sine wave to Preamp In Ch. 1 at P2-B22 (J7-2 or J5-2) and to Preamp In Ch. 2 at P1-C22 (J8-2 or J6-2). Measure the -3db point, using a scope, sync to external source. [Hint: -3db occurs when output drop from 5 div to 3.5div on scope.]

Circuit	Test Setup	Measure	Specification	Result
10 kHz filter (Channel 1)	Connect P1-B14 (or U17-8) to GND Connect P1-B15 (or U17-9), P1-B16 (or U17-16), P1-B17 (or U17-1) to +5V	TP7, U19-3	f_{-3dB}=10 ±0.1kHz	kHz
10 kHz filter (Channel 2)	Connect P1-B14 (or U18-8) to GND Connect P1-B15 (or U18-9), P1-B16 (or U18-16), P1-B17 (or U18-1) to +5V	TP8, U20-3	f_{-3dB}=10 ±0.1kHz	kHz
50 kHz filter (Channel 1)	Connect P1-B15 (or U17-9) to GND Connect P1-B14 (or U17-8), P1-B16 (or U17-16), P1-B17 (or U17-1) to +5V	TP9, U19-3	f_{-3dB}=50 ±0.5kHz	kHz
50 kHz filter (Channel 2)	Connect P1-B15 (or U18-9) to GND Connect P1-B14 (or U18-8), P1-B16 (or U18-16), P1-B17 (or U18-1) to +5V	TP10, U20-3	f_{-3dB} =50 ±0.5kHz	kHz
100 kHz filter (Channel 1)	Connect P1-B16 (or U17-16) to GND Connect P1-B14 (or U17-8), P1-B15 (or U17-9), P1-B17 (or U17-1) to +5V	TP11, U19-3	f_{-3dB}=100 ± 1kHz	kHz
100 kHz filter (Channel 2)	Connect P1-B16 (or U18-16) to GND Connect P1-B14 (or U18-8), P1-B15 (or U18-9), P1-B17 (or U18-1) to +5V	TP12, U20-3	f_{-3dB}=100 ± 1kHz	kHz
500 kHz filter (Channel 1)	Connect P1-B17 (or U17-1) to GND Connect P1-B14 (or U17-8), P1-B15 (or U17-9), P1-B16 (or U17-16) to +5V	TP13, U19-3	f_{-3dB}=500 ± 5kHz	kHz
500 kHz filter (Channel 2)	Connect P1-B17 (or U18-1) to GND Connect P1-B14 (or U18-8), P1-B15 (or U18-9), P1-B16 (or U18-16) to +5V	TP14, U20-3	f_{-3dB}=500 ± 5kHz	kHz

3.11 A/D Driver Gain Circuit

This tests the AD843 drivers U19 and U20 which drive the detector signal to the ADC.
Install J3, J4, J13, J14, J15, J16, J21, J22. Remove J1, J2, J9, J10, J11, J12, J17, J18, J19, J20.
Set Postamp gain to 1 by connecting P1-B18 (or U7-1) to GND and P1-B19 (or U7-16), P1-B20 (or U7-8), P1-B21 (or U7-9) to +5V for channel 1. For Postamp Gain =1 Channel 2, connect P1-B18 (or U8-1) to GND, and P1-B19 (or U8-16), P1-B20 (or U8-8), P1-B21 (or U8-9) to +5V.
Set Bandwidth to 500kHz for channel 1 by connecting P1-B17 (U17-1) to GND and P1-B14 (or U17-8), P1-B15 (or U17-9), P1-B16 (or U17-16) to +5V. For 500kHz channel 2, connect P1-B17 (or U18-1) to GND and P1-B14 (or U18-8), P1-B15 (or U18-9), P1-B16 (or U18-16) to +5V
Apply a 250±25mVp-p, 1.0±0.1kHz sine wave to Preamp In Ch. 1 at P2-B22 (J7-2 or J5-2) or Preamp In Ch. 2 at P1-C22 (J8-2 or J6-2).
Measure the gain at AD#1 and AD#2 using a scope, sync to external source.

Measure	Specification	Result
Voltage at AD#1 ("ANALOG TP A" on front panel) Ch. 2	1.0±0.2 vP-P	v
Voltage at AD#2 ("ANALOG TP B" on front panel) Ch. 1	1.0±0.2 vP-P	v

3.12 Reset Circuit
This test verifies the correct operation of the MAX810 reset IC (U37).
Apply +5v* to P3- 18 and CGND to P3-17.

Test Setup	Measure	Specification	Result
Adjust +5v P.S. down to +2.9 ± 0.1vdc.	TP19	+2.9 ± 0.3 VDC	VDC
Adjust +5v power supply up to +5.0 ± 0.1vdc	TP19	+0.2 ± 0.2 VDC	VDC
Turn +5v p.s. off and on again. Measure high period before goes low using a scope sync to +5v p.s.	TP19	stay high for 200 ±100 mSec	ms

3.13 Digital Multiplexer Circuit

This test verifies that the multiplexers U23 through U26 and the ISO150 isolators U27A through U34B are functioning properly.
Apply a 500kHz, square wave (0 to +5v) TTL pulse to TP17. Apply +5v* to P3- 18 and CGND to P3-17.
Verify that the output TTL signal is in correct phase with the input TTL signal.
U21Sim Switch and U22Sim Switch are circuits which connect pins 27 through 42 of each ADC to either AGND or +5V, controlled by a switch. These switches are installed in place of the actual ADC IC's U21 and U22.

Test Setup	Measure	Verify
Set U21Sim switch to "0" position Set U22Sim switch to "1" position.	Measure P3-2 through P3-6, P3-11 through P3-15, P3-19 through P3-24	TTL, In Phase?____
Set U21Sim switch to "1" position Set U22Sim switch to "0" position	Measure P3-2 through P3-6, P3-11 through P3-15, P3-19 through P3-24	TTL, Out of Phase?____
Set U21Sim switch to "0" position Set U22Sim switch to "0" position Turn +5v p.s. OFF and then ON.	Measure P3-2 through P3-6, P3-11 through P3-15, P3-19 through P3-24	0.0 ± 0.5 VDC_____