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NIRSPEC Electronics Application Note 5.00
DAQ17 Description

1 Introduction

The DAQ17 transputer board performs two functions. It is used as the clock generator for the infrared arrays, and it also has multiple parallel I/O ports which can be used for stepper motor driving, switch sensing and general digital control and monitoring. The DAQ17 was designed and built by DSP Systems, and evolved from two boards on the Gemini twin-channel infrared camera, the motor controller and the clock generator. These two boards were so similar architecturally it seemed reasonable to combine them, especially since this could be done within the real estate of a 6U VME board. The I/O ports were designed for motor control functions, but we also use them for auxiliary functions on the boards used for clock generation. Another advantage of combining the two boards is more efficient provision of spares. Combining these two board types reduces the number of transputer boards we have to spare to two.

2 Functional description

Each DAQ17 board has one T805 Transputer running at 25 MHz, with 4 MBytes of RAM. Logic programmed into Field Programmable Gate Arrays (FPGAs) is used to interface the CPU to I/O functions. Various registers are mapped into the memory space of the processor, so that writing or reading digital data is as simple as assigning or copying a variable. The logic can also interrupt the processor when needed for synchronization of events. Details of this process are also explained from the software side in NSPN18.

For clock generation, the DAQ17 transputer writes out via two 16 bit wide FIFO buffers with software selectable speeds. These FIFOs feed two output connectors, and the eight least significant bits are also copied to pins on the VME backplane so they can be passed to the acquisition boards (in our application we only use one of these lines). The FIFO output buffers are used in a repeating mode to take advantage of the repetitive nature of the clock waveforms for detector arrays. Data which isn't repetitive (usually start and end sequences) can be written to the output through a direct register, bypassing the FIFO buffers. The FIFO buffers can be run separately but we always run them synchronized.

In addition to the clock outputs, each board has four 8 bit output ports, the "motor" ports, and four 8 bit input ports, called ?status" ports. These come out on four DB25 connectors, one motor and one status port together on each. The status ports are always inputs, but the motor ports can be modified to act as bidirectional ports if needed.

The motor port output can be automatically terminated by a "watchdog" timer; this sets the output on the motor port to all zeros. One of the bits controls the power on/off line of each API stepper motor driver; a zero puts the driver into standby mode and powers down the stepper motors. This is vital in a cryogenic application as we want to minimize heat input into the instrument. For the same reason, the motor port bits also default to the off state when we power up the boards.

In addition to the transputer, its memory, and the I/O logic, there was room on the board to put in a dual TRAM[1] slot for the addition of off-the-shelf transputer interface modules.

3 System implementation

In the NIRSPEC electronics system, we use two DAQ17 boards for clock generation in the spectrometer and slit-viewing cameras. As well as producing clock pulses via the clock outputs, they control serial DACs and pre-amp gain and filter bandwidth though their digital I/O ports.

We use three more DAQ17s for motor driving, where they generate step pulses and direction, power on/off and high/low power signals, which are fed from the digital I/O ports to the motor driver modules. Microswitches in the mechanisms are fed back to the status inputs so the transputer code can figure out where the mechanisms are.

We also use one DAQ17 as the “root” transputer, which routes messages between the host computer and the rest of the transputer system. It also does some simple functions such as monitoring cabinet temperatures and controlling and monitoring the calibration unit lamps. This transputer board is housed in a separate “housekeeping” enclosure along with two RS232 TRAM modules, which interface to a computer-controllable power strip and the cryogenic temperature controllers and readouts. This one DAQ17 board is the only one that needs to be altered before being substituted with a spare, since one of the digital I/O ports has been modified to give it bidirectional capability for the cabinet temperature reading function.

4 Board layout and pinouts

4.1 Summary

The board is laid out in 6U VME format. Although it is used in a VME crate, it doesn’t use any of the VME bus lines, except for 5V power and ground. This allows us to use standard VME card cages and backplanes to package our transputer systems. Also, the VME bus has many uncommitted pins on the J2 connector, which we use for our system interconnects (serial links and control signals). The wire wrapping on the backplane is described in NEAN13.

[1] TRansputer Application Module - a standard daughterboard format for transputers packaged with various kinds of interfacing such as RS232 or SCSI.

The front panel of the DAQ17 is double the width of the DAQ15, and has 3 pairs of DB25 connectors and a pair of BNC connectors. The clock output ports are at the top of the panel on two side-by-side DB25 female connectors. Most bits of the clock output go from one of these DB25 connectors to the level shifter modules housed under the dewar, where they are converted to the voltage levels needed by the two different types of IR detector arrays. The eight least significant bits are also copied to the backplane connector J2. We use just one of these bits, as the `fifo.write` bit of the output waveform. It tells the FIFO input buffers of the DAQ15 acquisition boards to read in the next set of pixel values.

Two more clock bits are also wired to the two BNC connectors on the front panel. These two are used as the `convert` and `select` signals to the pre-amp/A-D boards. The `convert` pulse tells the A-D converters to convert the next set of pixel signals, and select (a level rather than a pulse) determines which of the two multiplexed A-D outputs is fed to the front panel.

The four digital I/O ports are on two pairs of DB25 male connectors. These are labeled 1 through 4. They are all identical.

4.2 Link speed selection

The speed of transputer serial links is selectable. The link speed for all the transputers on the board is controlled by a group of three switches, labeled S1, allowing 8 possible speed combinations. Link speed for the 0 link of all four transputers is set separately from links 1, 2, and 3. The speed for each setting of the three S1 switches is listed below.

Link0	20 MHz	20 MHz	10 MHz	10 MHz	10 MHz	10 MHz	5 MHz	5 MHz
Link123	20 MHz	10 MHz	20 MHz	10 MHz	10 MHz	5 MHz	10 MHz	5 MHz
S1A	off	off	off	off	on	on	on	on
S1B	off	off	on	on	on	on	off	off
S1C	off	on	off	on	on	off	on	off

Table 1 Link Speed Switch Settings

4.3 Backplane connections

The DAQ17 has two 96 pin DIN connectors (J1 and J2) at the rear of the board. Two rows of J2, J2A and J2C, are used for the transputer link connections. Each transputer has links 0 through 3, and a line for each direction (in or out). Signal LinkOut1 is therefore the output line of link 1.

There are also three “subsystem” signals, called error, reset and analyze, which are used by the transputers to form a system. The host computer for instance can assert the reset line to reboot all the transputers. These subsystem signals are bussed between all the transputers. Note that while the pinouts look similar to the DAQ15, the DAQ17 pinouts are actually quite different. Coupled with the wire wrapping of the network, this means the two board types can not be swapped!

In the table below, you will note there are three complete sets of links and two sets of subsystem signals listed. The links on the A column are for the DAQ17's on-board transputer, while the others connect to the dual TRAM sockets to connect any transputers plugged into there. The subsystem signals on A30-A32 are also for the primary transputer, while those on A27-A29 connect to the TRAM site. Spl0 - Spl7 are the eight least significant bits of the clock output, which are also seen at the front connector.

	J2A	J2C	
1	ground	ground	
2	unused	unused	
3	LinkOut1	LinkOut1	These are for the TRAM site furthest from the board edge.
4	LinkIn1	LinkIn1	
5	ground	ground	
6	ground	ground	
7	unused	unused	
8	LinkOut2	LinkOut2	
9	LinkIn2	LinkIn2	
10	ground	ground	
11	LinkOut0	LinkOut0	
12	LinkIn0	LinkIn0	
13	LinkOut3	LinkOut3	
14	LinkIn3	LinkIn3	
15	unused	unused	
16	ground	ground	
17	unused	ground	
18	Spl0	unused	
19	Spl1	LinkOut1	These are for the TRAM site nearest the board edge.
20	Spl2	LinkIn1	
21	Spl3	ground	
22	Spl4	ground	
23	Spl5	unused	
24	Spl6	LinkOut2	
25	Spl7	LinkIn2	
26	unused	ground	
27	notSubReset	LinkOut0	
28	notSubAnaylse	LinkIn0	
29	notSubError	LinkOut3	
30	nReset	LinkIn3	
31	nAnaylse	unused	
32	nError	ground	

Table 2 DIN-96 Link pinouts.

4.4 Digital I/O Ports

The DAQ17 uses two Field Programmable Gate Arrays (FPGAs) to map 32 bits of input and 32 of output to the transputer's memory space. They are split over four DB-25 male connectors, 8 bits of input and 8 bits of output on each. Each connector also has +5V and ground, which can be used to power remote ISO150 isolators. The output data bits are labeled MDD0 through MDD31 and the

input data bits are labeled SD0 through SD31. The connectors are stacked pairs on the double-wide front panel, and are labeled P1A, P1B, P2A and P2B on the board and Digital I/O 1 through 4 on the front panel.

Pin#	P1A	P2B	P2A	P2B
1	MDD0	MDD8	MDD16	MDD24
2	MDD2	MDD10	MDD18	MDD26
3	MDD4	MDD12	MDD20	MDD28
4	MDD6	MDD14	MDD22	MDD30
5	GND	GND	GND	GND
6	+5V	+5V	+5V	+5V
7	SD0	SD8	SD16	SD24
8	SD2	SD10	SD18	SD26
9	SD4	SD12	SD20	SD28
10	SD6	SD14	SD22	SD30
11	GND	GND	GND	GND
12	+5V	+5V	+5V	+5V
13	nPortOE0	nPortOE1	nPortOE2	nPortOE3
14	MDD1	MDD9	MDD17	MDD25
15	MDD3	MDD11	MDD19	MDD27
16	MDD5	MDD13	MDD21	MDD29
17	MDD7	MDD15	MDD23	MDD31
18	GND	GND	GND	GND
19	+5V	+5V	+5V	+5V
20	SD0	SD9	SD17	SD25
21	SD2	SD11	SD19	SD27
22	SD4	SD13	SD21	SD29
23	SD6	SD15	SD23	SD31
24	GND	GND	GND	GND
25	+5V	+5V	+5V	+5V

Table 2 DAQ17 I/0 Connector pinouts.

4.5 Clock output ports

The DAQ17 has two 16 bit wide by 16k deep FIFO output buffers, which can be used independently or as a single 32 bit by 16k FIFO. The FIFOs can be clocked at up to 50 MHz; this rate can be controlled via software. The FIFO data appears on two stacked DB-25S female connectors. When looking at the front of the DAQ17, the left DB-25 (Clock Out 1) supplies the lower 16 bits of the FIFO data. The upper 16 bits appear on Clock Out 2. The lower 8 bits (DataOut0 - DataOut7) of the data stream are buffered and redirected to the backplane, where they appear as Spl0 - Spl7 on the 96 pin DIN connector, J2a. The Splx bits are a duplicate of the bits on the front connector. These bits can be used to pass signals along the backplane, since they all go to

uncommitted pins on the J2 connector. In this application we use DataOut7 as the DAQ15 FIFO Write signal, which tells the DAQ15s to read in each set of pixel data from the A-D converters.

The A-D Convert and A-D Select bits are also generated as part of the clock waveform, as DataOut16 and DataOut18. They are brought out to two BNC connectors on the front panel, and from there go to the Interface board in the analog crate. We chose these particular data bits for convenience in picking off the signals from the back of the stacked DB25 connector (they also appear on the DB25).

The pinouts for the two DB25 connectors are given below.

Pin#	**Clock Out 1**	**Clock Out 2**
1	DataOut0/Spl0	DataOut16
2	DataOut2/Spl2	DataOut18
3	+5V	+5V
4	DataOut4/Spl4	DataOut20
5	DataOut6/Spl6	DataOut22
6	+5V	+5V
7	DataOut8	DataOut24
8	DataOut10	DataOut26
9	+5V	+5V
10	DataOut12	DataOut28
11	DataOut14	DataOut30
12	+5V	+5V
13	CONNSIG	CONNSIG
14	DataOut1/Spl1	DataOut17
15	DataOut3/Spl3	DataOut19
16	GND	GND
17	DataOut5/Spl5	DataOut21
18	DataOut7/Spl7	DataOut23
19	GND	GND
20	DataOut9	DataOut25
21	DataOut11	DataOut27
22	GND	GND
23	DataOut13	DataOut29
24	DataOut15	DataOut31
25	GND	GND

5 Schematics

DSP systems supplied some schematics with the boards. They are supplied along with this document, and listed below. There are 10 sheets.

Sheet #	Subject
1	Processor, link connections, processor speed jumpers.
2	Links on J2 connector and TRAM connectors J3 - J6, power & ground on J1 & J2B
3	Memory decoding FPGA.
4	FIFOs.
5	Memory.
6	Link speed switches, subsystem signals.
7	Digital I/O (motor/status) FPGA.
8	Digital I/O (motor/status) ports buffering details.
9	Clock output FPGA, output pinout, spl0-spl7 buffering and pinout.
10	Decoupling capacitors.

6 I/O port details

Each of the I/O port FPGA (labeled **Daq17_2.tdf** and **Daq17_3.tdf** on the schematics, page 7 of 10) handles 16 bits of I/O data. The Motor output bits (MDD0 - MDD31) are buffered by 7438 TTL open collector buffers. The outputs of the 7438s have pullup resistors and lead directly to the output connectors. In this configuration, a port can **only** be used for output, with high current drive capability. See page 8 of 10 of the schematics for the 7438 locations.

Since the 7438 is a unidirectional buffer, the output port cannot be used as a bidirectional port (or an input port) without a simple hardware modification. Removing the 7438 allows the FPGA output bits to be used as an input port. To reduce the risk of damaging the FPGA, the 7438 **must** be replaced by an inline resistor pack (labeled SIP4ISO-33, RP9 - RP16).

The 7438 is a 4 bit device, so there are 8 of them on the board. Since there are 32 output bits, each port can be used as an:

- 8 bit output port
- 8 bit input (or bidirectional) port
- 4 bit output, 4 bit input (or bidirectional) port

In every case but one, we only use the motor bits as output-only ports. The exception is where we drive Dallas Semiconductor DS1820 temperature sensors from the DAQ17 in the housekeeping enclosure (the crate above the power strip with the power strip legend on the front). One 7438 has been removed and replaced with a SIP resistor pack. **This modification must be taken into account when putting a spare board in place.**

The status port bits share the same connectors as the motor output bits. They can't be changed in any way and are always input only.