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December 16, 1998

NIRSPEC Electronics Application Note 04.00

DAQ15 Transputer Board Description

1 Introduction and functional description

The DAQ15 is the NIRSPEC data acquisition board, which takes in data from the pre-amp/A-D boards in the analog crate. Each DAQ15 board has four T805 transputers, running at 25 MHz, with 4 MBytes of dynamic RAM per transputer. Each transputer has its own logic for acquiring data from its front panel connector, so there are four independent acquisition systems on a board. We generally have all four subsystems doing the same thing using the same transputer code, although in the slit-viewing camera (SCAM) we only use two transputers on one board, and the other two transputers don't even have any network connection or run any code.

2 System implementation

The two camera channels have different IR array detectors with different numbers of output channels, so their requirements and system layouts are different.

2.1 Spectrometer channel

The 1024^2 Aladdin detector array has 32 analog outputs, which go to 16 dual-channel pre-amp/A-D boards (described in NEAN06). Each pre-amp/A-D board has two analog amplifier/filter chains, feeding 16 bit A-Ds. Under the control of the DAQ17 clock generator board, the A-Ds convert the analog signal. The digital outputs of the two A-Ds on each board are fed to a single output connector, which connects to an input connector on a DAQ15. Again under the control of the DAQ17 board, only one of the 16 bit output words is present at the front panel output at any time. With four transputers reading this multiplexed data, each DAQ15 board can service eight A-Ds, so this channel needs four DAQ15 boards, acquiring data under the control of its clock generator board.

2.2 Slit-viewing camera (SCAM) channel

The PICNIC array in the SCAM has only four outputs, so this channel has only 2 dual channel pre-amp/A-D boards, each of which feeds its multiplexed data to a DAQ15 input connector. This means we only need two of the four input subsystems on the DAQ15, so the transputer system for this channel is just one DAQ17 clock generator board and one DAQ15 acquisition board.

3 Board layout and pinouts

3.1 Summary

The board is laid out in 6U VME format. Although it is used in a VME crate, it doesn't use any of the VME bus lines, except for 5V power and ground. This allows us to use standard VME card cages and backplanes to package our transputer systems. Also, the VME bus has many uncommitted pins on the J2 connector, which we use for our system interconnects (serial links and control signals). The wire wrapping on the backplane is described in NEAN13.

On the front panel there are four DB26 high-density connectors where the 16 bit data come in. The four transputers, their memory and their input logic are in 4 identical sections behind the four input connectors. The four transputers on the DAQ15 can be easily identified. Transputer A is U1 and is near the top edge of the board when it is plugged into the backplane. Transputer D is U4 and is near the bottom edge. Transputer B is U2 and Transputer C is U3.

The transputers on all the transputer boards are interconnected using transputer serial links. These links are bidirectional and run at TTL levels over short distances. Both our types of transputer boards have their links connected through the DIN connectors on the VME backplane, using some of the uncommitted pins on J2.

Also coming in through J2 are two signals called Sync1 and Sync2. These can be used to trigger reading of data by the FIFO buffers. There is also a line called FifoClk in the front panel input connectors which can be used to trigger input. There are jumpers for each transputer, which select whether its trigger signal is FifoClk from the front panel or Sync1 or Sync2 from J2,.

Note: It is vital that you make sure the link speed dip switch and jumper selections are the same on any spare DAQ15 board that you substitute in to the system when troubleshooting, otherwise it won't work.

3.2 Link speed selection

The speed of transputer serial links is selectable. The link speed for all the transputers on the board is controlled by a group of three switches, labeled S1, allowing 8 possible speed combinations. Link speed for the 0 link of all four transputers is set separately from links 1, 2, and 3. The speed for each combination of the three S1 switches is listed below.

Link0	20 MHz	20 MHz	10 MHz	10 MHz	10 MHz	10 MHz	5 MHz	5 MHz
Link123	20 MHz	10 MHz	20 MHz	10 MHz	10 MHz	5 MHz	10 MHz	5 MHz
S1A	off	off	off	off	on	on	on	on
S1B	off	off	on	on	on	on	off	off
S1C	off	on	off	on	on	off	on	off

Table 1 Link Speed Switch Settings

3.3 Backplane connections

The DAQ15 has two 96 pin DIN connectors (J1 and J2) at the rear of the board. Two rows of J2, J2A and J2C, are used for the transputer link connections. The last letter after each link name indicates which CPU they apply to. Each transputer has links 0 through 3, and a line for each direction (in or out). Signal LinkOut1a is therefore the output line of link 1 of transputer A.

There are also three “subsystem” signals, called error, reset and analyze, which are used by the transputers to form a system. The host computer for instance can assert the reset line to reboot all the transputers. These subsystem signals are bussed between all the transputers. To control the reading of data into the input connectors, two lines called Sync1 and Sync2 come via the backplane from the clock generator board. A pulse on one of these lines can trigger the reading of a word of data through the front panel connector. We only use Sync1, since we trigger all the inputs together.

	J2A	**J2C**
1	ground	ground
2	unused	unused
3	LinkOut1a	LinkOut1c
4	LinkIn1a	LinkIn1c
5	ground	ground
6	ground	ground
7	unused	unused
8	LinkOut2a	LinkOut2c
9	LinkIn2a	LinkIn2c
10	ground	ground
11	LinkOut0a	LinkOut0c
12	LinkIn0a	LinkIn0c
13	LinkOut3a	LinkOut3c
14	LinkIn3a	LinkIn3c
15	unused	unused
16	ground	ground
17	unused	unused
18	LinkOut1b	LinkOut1d
19	LinkIn1b	LinkIn1d
20	ground	ground
21	ground	ground
22	unused	unused
23	LinkOut2b	LinkOut2d
24	LinkIn2b	LinkIn2d
25	ground	ground
26	LinkOut0b	LinkOut0d
27	LinkIn0b	LinkIn0d
28	LinkOut3b	LinkOut3d
29	LinkIn3b	LinkIn3d
30	notSubReset	Sync1In
31	notSubAnaylse	Sync2in
32	notSubError	spareInt

Table 2 DIN connector pinouts

3.4 Front panel input connectors

The DAQ15 has four high density DB-26 female connectors. Each connector feeds the 16 bit multiplexed data from a pre-amp/A-D board into a 16 bit wide, 512 word deep FIFO composed of two 8 bit wide Cypress 7201 FIFOs. Each 16 bit wide FIFO pair feeds 16 bits of multiplexed data into a single transputer.

These connectors also have a +5V supply line which goes to the analog boards. The digital output from each analog board is isolated from the transputer system using Burr-Brown ISO150 capacitive isolator chips. The transputer sides of these isolator chips are on their own separate ground plane area just behind the front panel, and the +5V from the DAQ15 boards powers the digital side of the isolators.

A Field Programmable Gate Array (FPGA) between the FIFOs and the transputers implements mapping of the FIFOs into the memory space of the transputers. This makes the programmer's job relatively easy. Reading data is simply a matter of copying it from one memory location (mapped to the FIFO) to another (in real memory).

It is important to note that the DAQ15's transputers **do not** control the flow of data from the A/Ds into the FIFO buffers. The FIFOs are triggered to read in the next value by an external write signal from the clock generator board.

1 ground	14 D10
2 D2	15 D13
3 D5	16 ground
4 D8	17 ground
5 D11	18 +5
6 D14	19 D0
7 ground	20 D3
8 +5	21 D6
9 +5	22 D9
10 ground	23 D12
11 D1	24 D15
12 D4	25 FifoClk
13 D7	26 10k resistor to ground, unassigned

Figure 3 FIFO Input Connector Pinouts

Note that in the above pinout, D0 is the least significant bit (LSB) of the A-D data and D15 is the most significant bit (MSB). The A-D converter data sheet defines its pin D15 as the LSB and D0 as the MSB. This has been corrected in the A-D board layout so that D0 on the DB-26 connector on the A-D board is the LSB, matching what the DAQ15 (and the rest of the world) expects to see. This is only significant if you need to look directly at the data coming out of the A/Ds.

3.5 Jumpers

The only jumpers on the DAQ15 board determine which external input pins trigger data taking. The reading of data into the FIFO input buffers must be clocked externally. This is done via either the backplane or the front panel input connectors. On the backplane, input pulses can come through on either the Sync1 or the Sync2 pin, on the J2 connector. On the front panel connectors the signal is called FifoClk. In the NIRSPEC system (both camera channels), we always get the pulses through Sync1 on J2, which is wire wrapped along the backplane to an output pin on the DAQ17 clock generator board.

Sync1 is on pin J2C-30 and Sync2 is on J2C-31 of the backplane connector. FifoClk is on pin 25 on the front panel DB26 connector.

To choose between front panel or backplane connector J2 for the FIFO read signal we use jumpers JP1 through JP4 (for transputers A through D). A jumper on pins 1 and 2 selects the front panel input, and 2 to 3 (default) selects the backplane.

To choose between Sync1 and Sync2 from J2, we use JP5 through JP8 (for transputers A through D). A jumper from 1 to 2 (default) selects Sync1 and a jumper from 2 to 3 selects Sync2.

4 Schematics

DSP systems supplied us with 19 sheets of the schematics for the chip. The contents are listed below.

Sheet #	**Subject**
1	Backplane connections
2 — 5	Transputers and associated jumpers
6 — 9	Addressing logic
10 — 13	Input connector pins, FIFO buffers and input control FPGA
14 — 17	DRAM
18	Jumpers, subsystem signal buffering and CPU clock
19	Bypass capacitors